MULTIFUNCTION DSP BASED REAL-TIME POWER QUALITY ANALYZER

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Abstract: In the paper, the design and implementation of a high-performance real-time power quality measuring instrument based on digital signal processor (DSP) is discussed. After the hardware and firmware instrument description, the paper continues with the presentation of power quality analyzer software design and then is completed with metrological characterization of the instrument prototype, in terms of measurement accuracy and speed of execution.

Keywords: real-time instrument, power quality index, DSP, digital measurement.

1. INTRODUCTION

Measurements and monitoring of low frequency conducted disturbances on electrical network (commonly addressed as power quality issue) are becoming more and more discussed topic because quality of energy will be one of the most important parameter in trading of energy in open market scenario. Unfortunately, at the moment, power quality (PQ) phenomenon definitions that can be found in different standards (f.i, IEC, IEEE, etc.) often aren't fully harmonized and several definitions for the same terms exist.

Before scheduling power quality measurement, the user must select the instrument which meets their needs. Without the assessment specification of the instrument, or with an inappropriate specification, users are unable to assess the severity level of the disturbance; this can lead to incorrect conclusions and costly decisions.

Main problems in definition of instrument characteristics came from the divergent requirements that different PQ analysis has. Typically some phenomena (such as transients) require a very fast analysis in short time interval, while others (such as flicker) are assessed over very longer time interval (10 minutes). Anyway, the monitoring should last for very long time interval (at least a week better a month or a year). Finally, monitoring points are far to reach or geographically distributed, the monitoring results should be accessible thought a telecommunication network.

The standards that give nearly close references to power quality phenomena are the IEC 61000 family. In particular the authors mainly refer to the standard 61000-4-30 [2] establishing the data acquisition attributes necessary to characterize different power quality phenomena. In order to address the monitoring standard requirements, a real time digital instrument, based on DSP architectures is proposed. A DSP developer board is the best choice to implement real-time PQ analyzer, which allows the monitoring of transients and steady state PQ disturbances, with high flexibility and with low cost. Instruments for real-time measurements are characterized by an absolute time constraint for input, processing and output operations accomplishing, which must not be exceeded. After the description of hardware design and implementation, the developed firmware, that adopts a second level boot for stand-alone operating mode, will be illustrated. Then, the software structure for integrated PQ indexes measurement will be presented. The paper will present also some characterization aspects of the instrument prototype, through preliminary experimental results.

2. INSTRUMENT DESCRIPTION

A simplified scheme of the proposed PQ analyzer is shown in figure 1. It is mainly composed by: i) a data processing block; ii) an acquisition block; iii) a communication front end.

The data processing block adopts the TMS320C6711 32-bit floating-point DSP, mounted on Developer Starter Kit (DSK) board, based on the very-long-instruction-word (VLIW) architecture. This processor perform 100 Mips and, thanks arward core architecture, allows, through two different memories, to manage instructions and data separately.

The data acquisition block allows the presence of three sections in order to condition, to sample and to convert, from analog to digital, the input signal. Measurements are carried out by current and voltage transducers, chosen in agreement with the standards. The two isolated signals are sent to the 12 bit A/D converter (THS1206) through two sample-and-hold circuits with a sampling rate up to 6 MS/s.

A 32-bit external bus interface(EMIF), directly connected with onboard DSK RAM, connects and manages the data flow between processing unit and data acquisition system and between processing unit and web server. The communication front end is composed by the HD1200 web server device has the task of implementing the TCP/IP protocol. This device communicates directly with the DSP through a Dual-Port RAM (DPR), utilized as memory buffer
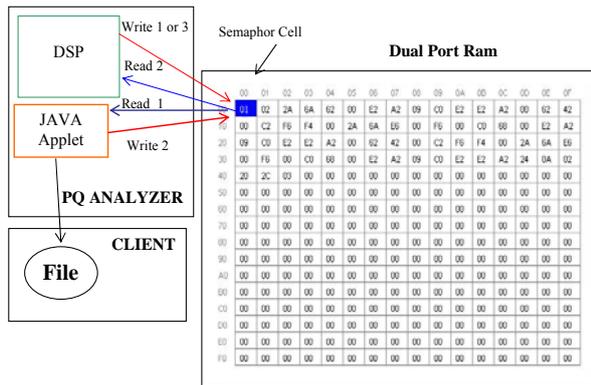
Fig.1: Real time instrument block diagram

interface, and with a generic client by means of the network interface. The Joint Test Action Group (JTAG) interface is used, in order to implement the communication between target DSP and a PC host to permit the instrument control in emulation mode, the I/O instructions and the output data exchange. In particular, real-time data exchange channels (RTDX) on JTAG interface are used to implement the local data transfer. These channels allow transferring data between the digital instrument and a local PC without interfering with the target application.

2.1 Instrument firmware

The design and implementation of special purpose DSP system requires high costs and time spend. By using a general purpose DSK board, and by modifying opportunely its firmware, it is possible to realize a stand alone instrument with high performances and low cost.

Normally the DSK is used in Emulation Mode that needs the presence of PC controller. In order to utilize the instrument in stand alone mode a second level boot was implemented. It includes the possibility to restore the emulation mode in order to update purpose.

The second level boot, after DSP power-on, also perform a self test control on the configuration of DSP board switches. According with switches position the DSP runs the PQ

Fig.2 CCS second level boot debugger

algorithms in stand alone mode or passes the DSP management to PC in emulation mode. If the emulation mode is chosen, then the boot stops itself and the management is left to PC. At the starting of stand alone mode, under the release of the internal reset, 1 kByte of code is allocated in the starting address of the external memory block 1. This address corresponds to the starting address of the Flash memory and its content will be automatically copied in the correspondent address of the DSP second level cache. In figure 2 the boot code, for flash programming, in Code Composer Studio (CCS) debugger environment is shown. All these operations are made while the CPU is in halt status, by using the default timing of the ROM.

After the described transfer, the CPU exits the halt status and begins to execute the instructions from the memory address 0, by configuring some registries of the EMIF.

To store the boot code in DSP cache memory two operations are necessary. After that the boot code is compiled, the first step is that to convert object file from executable to hexadecimal file through a CCS HEX6X DOS-script. The second step is the hex code loading in the internal DSP cache memory. This operation can be made or with another CCS script said FLASH either with an opportunely assembler code.

2.2 Acquisition management

Every time that a signal sample is acquired, the ADC produces a "data available" signal that is sent to the DSP "hardware interrupt". When this interrupt occurs the data is passed from the ADC-FIFO to EMIF, directly connected with DSK RAM, through DMA controller supervisions. The DMA controller reads and manages the data until one of three data-buffers is full. When the buffer full occurs, the DMA stop the DSP process through an interrupt, changes the read buffer and exchange the archived data with DSP through an ISR-target application. All data acquisition and storage operations are made while the DSP executes the measurement algorithms. The data exchange trough DMA and DSP is made by respecting the processing time constraint.

2.3 Remote communications

In this section is described as the DSP and HD1200 web server interface has been implemented. The hardware interface was made through a DSP EMIF and a DPR available on the HD1200 board.

In the microweb server some HTML static pages are stored. These pages allow the possibility to communicate with client by mean of a browser. The HTML allows to create only static pages. To permit the DSP output data exchange in dynamic way, a JAVA applet, included in HTML page, has been created. To manage the HD1200 and the DSP communication, a DPR cell was been used as semaphore (see figure 3). In fact, when the cell is set to 1, the applet can read on DPR. After that, the applet has read the data block, it sets the cell to 2, permitting to the DSP to write the new values block. When the output data is ended, the DSP sets the cell to 3. In this condition the applet plots the data to client interface and wait the new data stream through a polling loop on DPR cell.

Fig. 3 DSP-Web server communication protocol

An optimization process has been performed in order to minimize the number of executable instructions necessary to implement the measurement algorithm. This has allowed to allocate all target program in DSP internal memory. The interrupt service routine (ISR) to reduce the time latency between data acquisition and data processing, has been employed by utilizing one of the twelve software interrupts available on DSP and by modifying the interrupt service table (IST) with the starting address of the target application. The DSP processes the data in continuous loop until the interrupt-application occurs.

3. MEASUREMENT ALGORITHMS

In the proposed instrument, specific algorithms for each one of PQ phenomenon are developed, referring to the standard IEC 61000-4-30 [2].

The power quality parameters considered in this standard are power frequency, magnitude of the supply voltage, flicker, supply voltage dips and swells, voltage interruptions, voltage transients, voltage and current harmonics and interharmonics.

The structure of the software instrument implementations is schematically shown in figure 4. In particular, in the figure, it is evidenced software part with hard real time constraints (Real Time Section) and the other part with looser time constraints (On-Line Section).

The samples are acquired with a sampling frequency of 1 MS/s and each sample is analyzed in order to detect transient phenomena (section A). The time domain algorithm adopted is fully described in [4]-[5]. This section is directly connected with a flagging event register.

So, samples are processed with a low-pass filter with 20 kHz cut-off frequency (section B), averaged and decimated in order to increase the resolution for the following analyses which require 9 kHz frequency band at last. The so obtained samples are buffered (section C) and the buffer is managed in dynamic way so that while half buffer is processed the other part keeps to be filled from incoming new samples. Of course elaboration time should be less than half block filling time. The block D is used to estimate the actual fundamental frequency in order to perform synchronized analyses. The section E individuates dips through rms continuous processing. A digital flickermeter is implemented in block

F. In the section G, at first a digital re-sampling is made to obtain in exactly ten cycle of the fundamental a number of samples that is always a power of two, accounting of power frequency fluctuations. In this way, a synchronized spectral analysis is performed with 5 Hz spectral resolution and harmonics and interharmonics groups can be properly calculated. The results of all the measuring sections are validated accounting the flagging concept [2]. It avoids counting a single event more than once in different parameters (for example, counting a single dip as both a dip and a frequency variation). In this case, the data is flagged and not accounted for subsequent analysis. Not flagged data are grouped with reference to absolute time in order to obtain measurement with absolute 10-min clock boundary.

3.1 Fundamental frequency detection

The accurate synchronization is essential to implement some analyses, according to reference standards, and to estimate the fundamental frequency deviation for a correct remodulation of the analysis window. Moreover the spectral leakage of fundamental component produces remarkable effects on all near harmonics and interharmonics groups. For this reason, the accurate synchronization represents a necessary operation. The synchronization of the input sequence is implemented by two main sections: i) hysteresis threshold block that selects a number of samples between
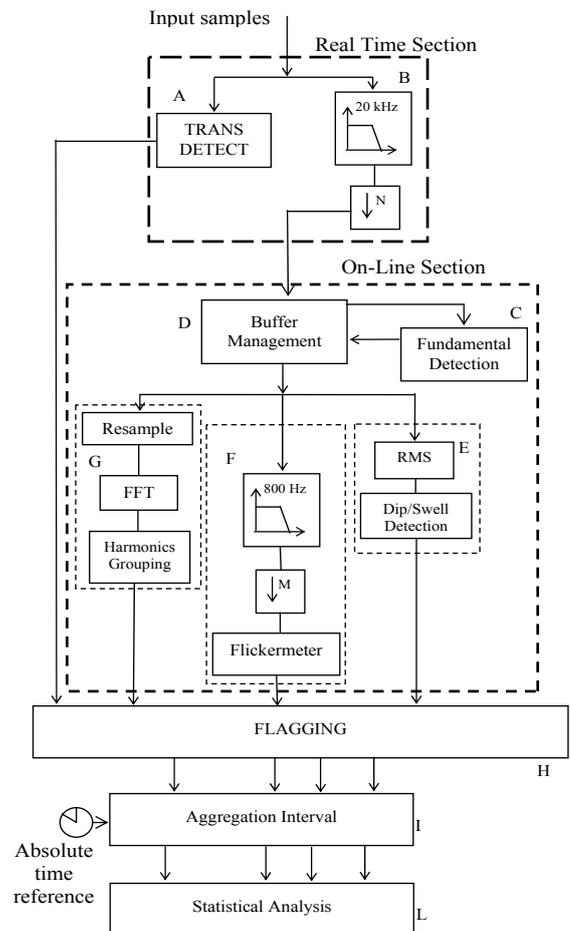

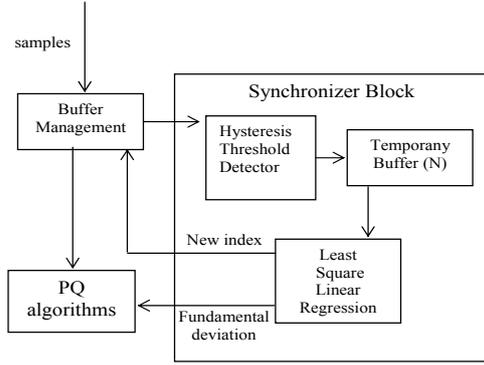**Fig. 4 Real Time software instrument implementation.**

Fig. 5 Synchronizer block diagram

Fig. 6 Frequency deviation

the first and the second zero crossing; ii) least square linear regression block, that rebuilds the real index position of the input samples zero crossing. The input samples are passed in a threshold hysteresis block, accumulate in a N dimensional buffer and finally are processed by a least-square linear regression algorithm. A part of synchronizer block is shown in figure 5. The square of the error between the measured points and the considered straight line equation is used to find the zero crossing index. By deriving the square error with respect to the straight line parameters, and by placing these terms to zero, it is possible to obtain the index value correspondent to zero crossing. This value, is given as a new starting index to the buffer management section and the fundamental deviation is given as a factor to remodulate the size of the window analysis. The value of the frequency is obtained by adopting the following mathematical relation:

$$fo = fc \frac{1}{(x(1) + \Delta x1 - x(0) - \Delta x0)} \tag{1}$$

where fo and fc are respectively, the fundamental estimate and the sampling rate, while $x(1)$ and $x(0)$ are the indexes values correspondents to the first and second zero crossing with added the respective $\Delta x1$ and $\Delta x0$ residuals.

In figure 6, is shown the relative error estimate from fundamental detection algorithm by using only ten elements. These measurements were obtained by applying single tones with frequency ranging from 42.5 Hz and 57.5 Hz at section C, and with initial phase comprised between 0° and 180°. The relative error doesn't exceed 0.15%. In particular working conditions, this error has some peaks, as when the fundamental frequency become below 45 Hz. In the other working conditions the error is always below 0.05%. In conclusion, linear least squares regression makes a very efficient use of the data. It allows good results, as is possible to show with only ten elements.

3.2 Rms algorithm

The algorithm for rms monitoring adopts a sliding window technique. It is based on the Eulero's equation for the rms calculation:

$$V_{RMS}^2 = \frac{1}{N} \sum_{i=0}^{N-1} v_i^2 \tag{2}$$

where N is the ratio between the sampling rate and the input signal frequency. The sliding window application to the (2),
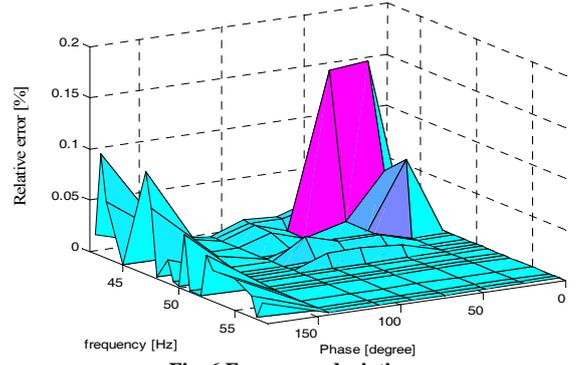
leads to:

$$V_{rms}^2(k) = V_{rms}(k-1)^2 + \frac{\left(V^2(k) - V^2(k-N+1)\right)}{N} \tag{3}$$

By adopting this technique, a new rms value is calculated each new sample acquired and only three numbers are processed. It is necessary, for the algorithm, to store N samples. For this reason a circular FIFO buffer has been used. Measuring rms in this way not only is compliant with the standards, but also can detect disturbances with a better time resolution. The errors, caused by the fundamental frequency deviation, are compensated through the modulation of factor N in equation (3) calculated with the fundamental frequency estimate in each period (eq. (1)). Over the analyses advantages due to rms instantaneous evaluation, referred to one period of fundamental, this method allows, after an initial transient of one period time duration, to store only four elements as shown in equation (3), by respecting the limited memory constraint.

3.3 Resampling

The resampling block allows to obtain the desired number of samples from the numeric sequence corresponding to 10 cycles of measured power frequency. This block is necessary because the section of harmonics and interharmonics grouping is composed by the FFT algorithm. So, after that a fixed 2^n value was chosen according to the highest frequency analyzable, it is possible to resample the original sequence, whichever is its length. The new samples are taken at non integer index corresponding to the following equation:

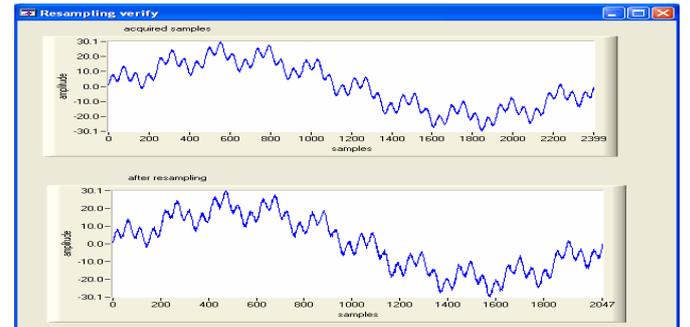$$k\alpha = k \frac{T_{10cycles} f_s}{2^n} = m_k.d_k \qquad \forall k = 1...2^n \tag{4}$$
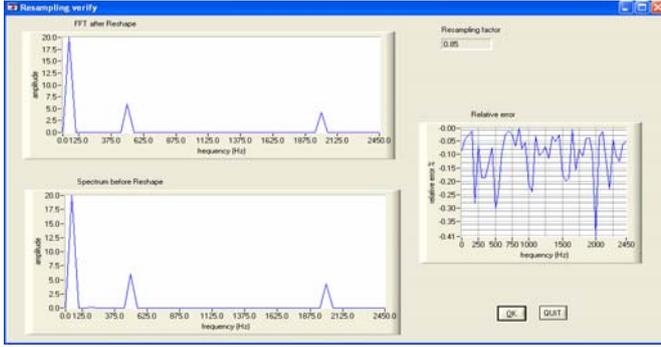

Fig. 7 Resampling input and output sequence

Fig. 8 Resampling algorithm relative error

where m_k and d_k are the integer and decimal part of the index corresponding to the k-th new sample, $y_R(k)$. $y(m_k)$ and $y(m_k+1)$ are the two consecutive samples adopted to calculate $y_R(k)$. d_k is the relative distance of $y_R(k)$ from $y(m_k)$. The value of new sample can be calculated as:

$$y_R(k) = y(m_k) + \Delta y = y(m_k) + \frac{d_k(y(m_k +1) - y(m_k))}{10} \quad (5)$$

To become the sequence analyzable in harmonic grouping section, the resampling algorithm change the sample rate from 12 kHz to 10.240 kHz. The figure 7 and the figure 8 show a test of realized resampling algorithm. In particular the algorithm has rebuilt an input signal formed by three tones at 50 Hz, 500 Hz and 2000 Hz with amplitude respectively of 20 V, 6 V and 4 V. After that, the spectral analysis on input and output sequence was made, the relative percent error has been valued. As it is possible to show in figure 8, the relative error doesn't exceed 0.5% up to 2 kHz, according to [3].

3.4 Harmonic Grouping

After an on-line FFT execution, the section H calculates harmonics and interharmonics groups. This grouping method provides an overall value for the interharmonic components between two discrete harmonics, which includes the effects of fluctuations of harmonic components [3]. This evaluation is made after that ten periods of fundamental have been acquired. This involves that the frequency step resolution is 5Hz as recommended in IEC 61000-4-7 standard.

4. EXPERIMENTAL RESULTS

In order to characterize the implemented measuring system, some experimental tests focalized to evidence the frequency domain analyses are reported. In particular, to implement a performances analysis of PQ analyzer with regards to harmonic analysis, is chosen a set of test according to [3]. The scope of these tests is to check the accuracy of implemented instrument in particular working conditions. In fact, the analytical results of harmonics and interharmonics grouping have to be compared with the output results of proposed PQ analyser.

4.1 Test station

The test station, adopted for performance verification of PQ analyzer, is composed by a signal generator, implemented in
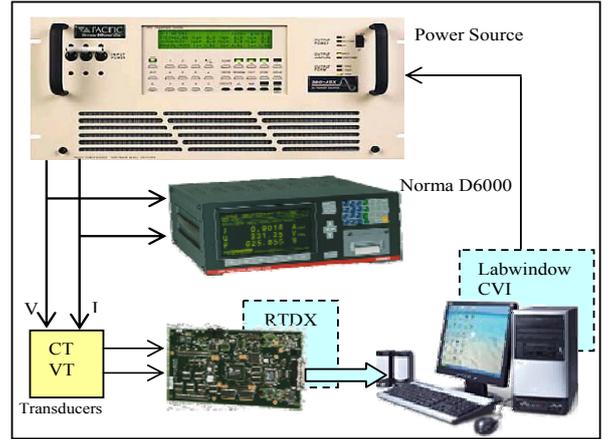

Fig. 9 Measurement Station

CVI environment, that drive a Pacific Power source, where a combination of harmonics and interharmonics tones are generated. The Norma D6000 is used to verify the signals generated. The measurement station is completed by the instrument under test, that perform PQ analyses, and by a personal computer, that receives results through RTDX channel and displays them. The results are plotted through an executable program on local PC developed in CVI platform. A simplified diagram of the station is reported in figure 9.

4.2 Tests results

Three test signals are implemented in order to verify the performance of instrument in the analysis of specific signals generated by non linear loads or by communication systems. The fundamental component is not considered as specified by reference standard [3].

In particular, the first generated signal is a communication signal, with interharmonic at 178 Hz and 23 V of amplitude, and two harmonics at 150 Hz and 250 Hz, with both amplitude of 11.5 V. The figures 10 a) show the acquired waveform, the 10 b) the signal spectrum and the 10 c) the harmonic and interharmonic subgroups for the test 1. In Table I the expected analytical values, the obtained results and the associated relative error are reported.

The second test signal is composed by the sum of three tones: 287 Hz communication signal with 9.8 V amplitude, 250 Hz harmonic with 13.2 V amplitude and 300 Hz harmonic with 10 V amplitude. The interharmonic subgroup has to be lower than 9.534 V[3]. The figures 11 a) show the acquired waveform the 11 b) the signal spectrum and the 11 c) the harmonic and interharmonic subgroups for the test 2. In Table II the expected analytical values, the obtained results and the associated relative error are reported for test 2.

Last test signal is the combination of two phenomena, the harmonics and interharmonics generated by an electronic motor drive with a varying torque (carrier harmonic at 250 Hz with 10 V amplitude and two interharmonics at 245 Hz and 255 Hz both with 1 V amplitude) and a communication signal with an amplitude of 9.8 V and frequency of 287 Hz. In the described test 5 Hz frequency spectral resolution plays a very important role in measurement of the interharmonic components.

In fact, interharmonics chosen are at frequencies that are not an integer multiple of spectral resolution, so they aren't directly "visible" to the FFT algorithm, because their periods aren't integer multiple of the analyzed time window. This limited resolution imply a spread of interharmonic spectrum on nearest spectral components even reaching harmonic groups. These tests have shown that the PQ analyzer error, on the spectral analysis, doesn't go beyond 1.2%, hence complies the value of the standard limits. Better results are attended with a more complex resampling algorithm but accounting of tradeoff with time constraint.

5. CONCLUSIONS

In this paper, the design and implementation of a high-performance real-time power quality measuring instrument based on digital signal processor has been discussed. In particular, after the description of hardware implementation,
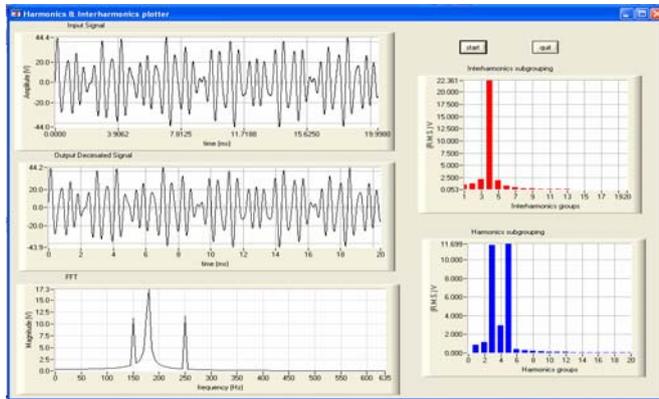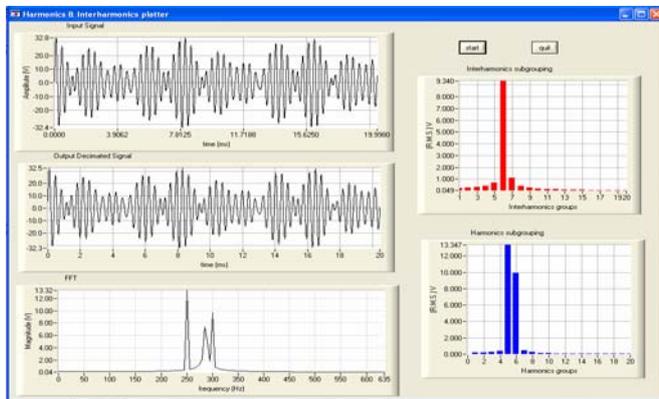

Fig.10 Test 1 PQ analyzer results
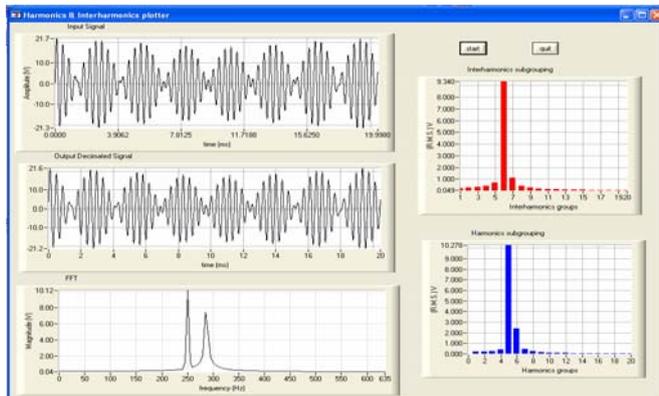

Fig.11 Test 2 PQ analyzer results

Fig.12 Test 3 PQ analyzer results

the developed firmware, that adopts a second level boot for stand-alone operating mode, has been illustrated. Then, a software structure for integrated indexes measurement was presented and tested generating some test signals according to IEC standard and comparing the measurement results of harmonic and interharmonic groups with expected analytical values. The performed tests have shown that the accuracy is compliance with the standard limits.

Table I - test 1 results

	4° interharmonic group	3° harmonic group	5° harmonic group
Expected values (V)	22.51	10.30-12.70	11.10-11.30
Obtained results (V)	22.36	11.70	11.40
Relative error (%)	-0.66	Within the range	0.89

Table II - test 2 results

	6° interharmonic group	5° harmonic group	6° harmonic group
Expected values (V)	9.53	13.20	10.00
Obtained results (V)	9.44	13.35	9.89
Relative error (%)	0.99	1.11	1.10

Table III - test 3 results

	6° interharmonic group	5° harmonic group
Expected values (V)	9.34	10.23
Obtained results (V)	9.43	10.28
Relative error (%)	0.96	-0.47

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