XVII IMEKO World Congress
Metrology in the 3rd Millennium
June 22−27, 2003, Dubrovnik, Croatia

IMPROVING DYNAMIC RESISTANCE AND DIFFERENTIAL CAPACITANCE MEASUREMENT OF ACTIVE DEVICES

Henrique Quaresma, António Pedro Silva, António Serra

IT/DEEC – IST, Universidade Técnica de Lisboa, Lisbon, Portugal

Abstract − A numerical model of a general purpose commercial equipment for current versus voltage (I-V) and differential capacitance versus voltage (C-V) measurement of active devices is presented. The good agreement between the model results and experimental data show that the model takes into account the main error sources of the instrument and can be used as a base to perform error correction and to implement a calibration procedure.

Keywords: dynamic resistance, differential capacitance, calibration method.

I. INTRODUCTION

A large number of new impedance measurement techniques have been developed in the last decade [1-5]. The accuracy of the results in many of those relies on powerful calibration procedures for systematic error correction. The availability of low cost and powerful Personal Computers allows the implementation of calibration techniques also in commercial measurement instruments where data is available in digital format and enough information exists to model the instrument.

In this paper we will present a numerical model that can predict the behaviour of a HP4140B during dynamic resistance measurement and consequently enabling the implementation of an error correction technique to improve the quality of the results. The application of this procedure to differential capacitance measurements by the same instrument is straightforward.

The model assumes that systematic errors are time invariant (and consequently predictable), can be characterized during a calibration process and mathematically removed during the measurement procedure.

During the electrical characterization of a new MOS device designed in our research group [6] a sophisticated HP4140B pA meter/DC voltage source was used to measure the dynamic resistance. Experimental results showed an unexpected trend. This was the motivation for the work here presented.

II. NUMERICAL MODEL

HP4140B is a pA meter with two DC programmable voltage sources. One of them being programmable as a voltage ramp is synchronized with the current measurement stage making possible accurate I-V and C-V measurements. The voltage source is able to generate voltage ramps from - 100 V to 100 V with a ramp rate varying from 0,001 V/s to 1 V/s. The instrument meter has ten current scales from 10^{-12} A to 10^{-2} A, including a 12 bits resolution successive approximation register Analog to Digital Converter (ADC). Analog current values are sampled at a 10 ms rate, digitised and stored in a Random Access Memory (RAM). After storage a digital integration technique is applied and its result is presented to the user.

The I-V measurement results obtained for our MOS device characterization were quite different from the expected ones. To validate those, the measurement system was verified by measuring discrete passive devices, such as precise resistive loads, that should present constant resistance values for all applied voltages and voltage rates. Three different resistive loads were measured: 99,5 Ω, 10 kΩ and 1 MΩ, such that almost all current scales of the equipment were verified.

The measurement procedure as described in [7], consists on applying a voltage ramp with user defined start and stop voltages, and a positive ramp rate (dV/dt). I-V data obtained at the end of the measurement procedure was used to calculate the absolute error of the measurement

$$\varepsilon_R(V) = V/I - R_S \tag{1}$$

with respect to the well known measured resistive load R_S. Results obtained were very different from the constant resistive value expected from Ohm's law. In Fig.1 one can see the absolute error for a 99,5 Ω resistive load, obtained by applying a voltage ramp varying from – 1 V to 1 V at rate of 0,005 V/s.

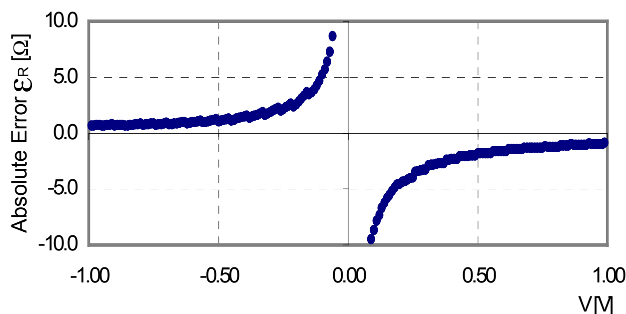


Fig. 1 – Experimental absolute error in the measurement of a 99,5 Ω resistance.

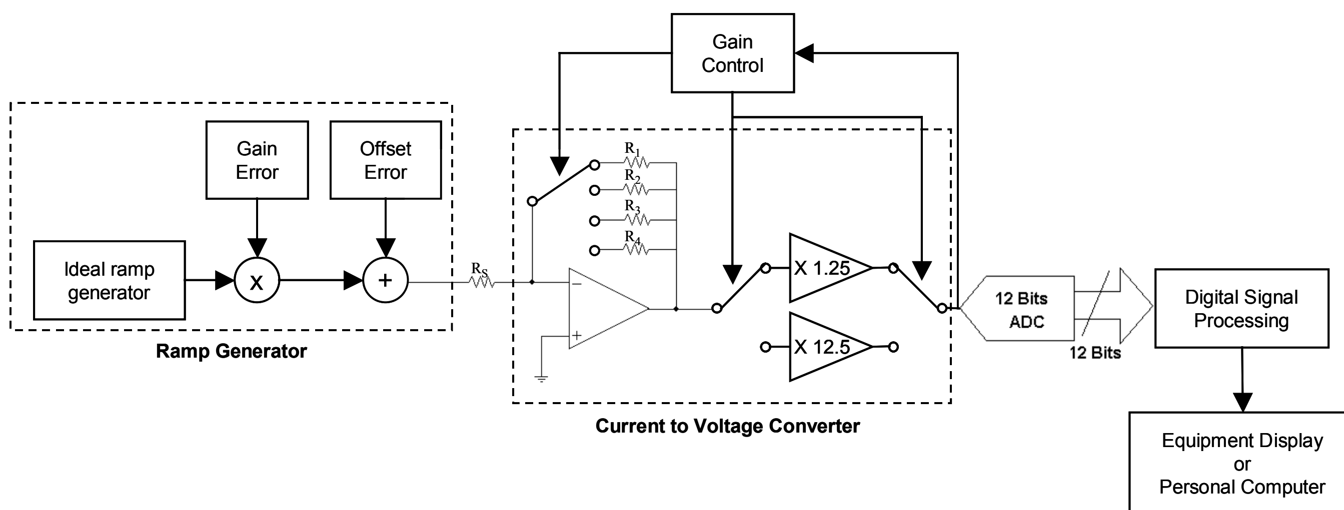


Fig. 2 – Block diagram of the numerical model of the instrument.

It can be seen that near origin error values tend to ±∞, and that when |V| increases the absolute error approximates zero.

The surprising results shown in Fig. 1 lead us to develop a numerical model of the HP4140B based on the instrument description [7], in order to understand what was going on and to be able to extract accurate measurement results from the instruments output. The block diagram of the model is presented in Fig. 2.

The voltage ramp generator block includes the modelling of gain and offset errors. These take into account the overall gain and offset errors in all the other blocks of the measurement circuit. The current to voltage converter including a gain circuit (of 1,25 or 12,5) converts every sampled current value I_S=y,yyy × 10^{-x} A to a proportional voltage within the range ± 2,5 V. The gain is automatically adjusted in such a way that independently of the current scale, 10^{-x}, the stimulation of the ± 2,5 V range is optimised. Following current to voltage conversion, the analog voltage values are digitised through an ideal 12 bits successive approximation ADC with local full scale of ± 2,5 V. After digitisation digital signal processing is performed every 10 ms, comprising a voltage to current conversion and a moving average procedure. The number of current samples considered in the moving average, depends of integration time and can vary from 2 to 256. Discrete voltage values and the correspondent averaged current values obtained from simulation are used to calculate R(V) values.

The amplifiers, the passive components and the switches included in the measurement circuit are considered ideal.

The first procedure to perform is the computation of gain and offset error values to use in the ramp generator block. These can be obtained from *n* experimental (I;V) pairs by minimizing the least square error:

$$J = \sum_{i=1}^{n} \left(I_i - \frac{1}{R} \left(V_i \times \text{Gain} + \text{Offset} \right) \right)^2 , \qquad (2)$$

where I_i is experimental current value and V_i is experimental voltage value.

The solution of this problem for gain and offset is respectively:

$$\text{Gain} = \frac{\sum_{i=1}^{n} I_i R V_i - \frac{1}{n} \sum_{i=1}^{n} \sum_{j=1}^{n} V_i I_j R}{\sum_{i=1}^{n} V_i^2 - \frac{1}{n} \sum_{i=1}^{n} \sum_{j=1}^{n} V_i V_j} \qquad (3)$$

and

$$\text{Offset} = \frac{\sum_{i=1}^{n} \left(I_j R - V_j \text{Gain} \right)}{n} . \qquad (4)$$

III. RESULTS

The absolute error in passive resistance measurements (1) was computed for numerical simulation results and for experimental data. Results were compared and it could be noticed that the tendency of two curves was similar, even if they did not fit. Fig. 3 shows results for the 99,5 Ω passive resistance measurement.

Trying to understand the differences between the results of our computational model and experimental data, we compared the I-V experimental data (available before resistance calculation) with I-V numerical simulation values. We found that the experimental current voltage curve presents a discontinuity when the voltage crosses zero. Different offset values for negative and positive voltages were noticed. This could be easily explained if different amplifiers were used to produce the positive and negative branches of the voltage ramp.

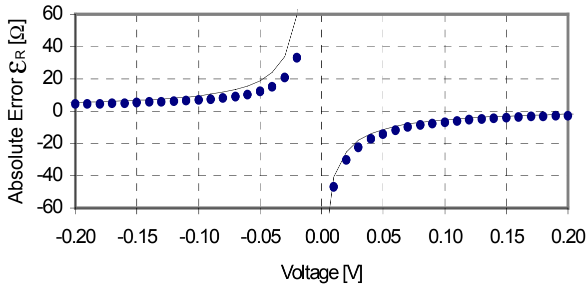


Fig. 3 – Resistance absolute error for a 99,5 Ω passive resistance measurement. Experimental (marks) and simulated data (line), after unique gain and offset correction on voltage source have been considered.

According to this, we decided to solve the least square problem for positive and negative voltages separately, obtaining different gains and offsets values for each one. When considering these parameters the new simulation results present an excellent agreement with experimental data, Fig. 4.

To validate the numerical model, the difference between experimental I-V and simulated I-V was computed and it is presented in Fig. 5. It can be seen that in the voltage intervals [-1; -0,2] V and [0,2; 1] V, the difference between experimental and numerical simulation results follows closely the quantization error of an ideal digitiser, even if some points are beyond the ± 0,5 LSB (Least Significant Bit) bound. These very small differences (less than ± 0,2 LSB) can be easily justified by 4 effects: (i) the lack of synchronism between experimental and simulation time sampling of the analog voltage ramp; (ii) the non linearity of the ramp generator (iii) the non ideal INL (Integral Non Linearity) of the ADC and (iv) the presence of noise inevitably present in any experimental setup.

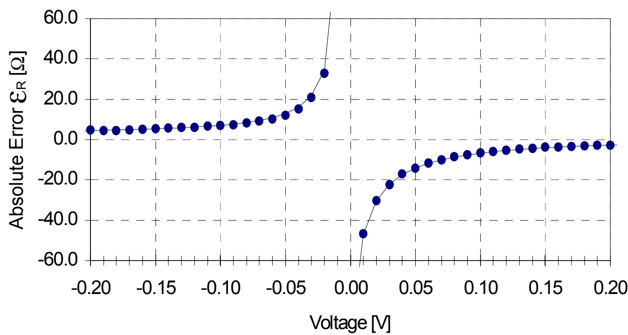


Fig. 4 –Same as in Fig. 3, after positive and negative voltage source offsets and gains have been considered.

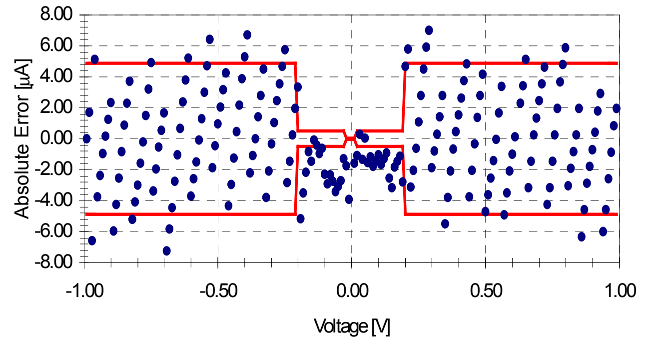


Fig. 5 – Difference between experimental I-V and simulated I-V data (marks), in the conditions of Fig.4. Solid lines represent the error bound for ± 0,5 LSB.

One can also see that the current scale changes near ± 0,2 V and ± 0,02 V. By zooming Fig. 5 in the interval ± 0,2 V, Fig. 6, we verify that the behaviour of the absolute error, no more can be justified by the quantization error. This should not be a surprise since the large increase on the resolution of the digitisation makes that the dominant source of error is now one of the four effects referred in the last paragraph. According to our experience on ADC testing [8] and since different records of experimental data show the same trend of the results of Fig. 6, probably the dominant source of error is now the non-linearity of the voltage ramp generator and/or the ADC non-linearity.

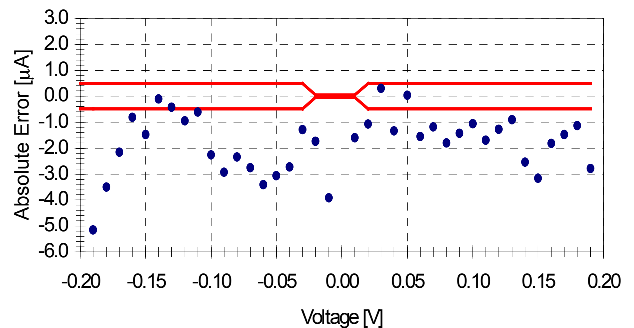
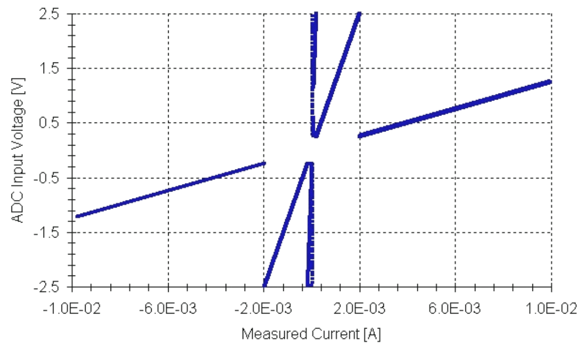
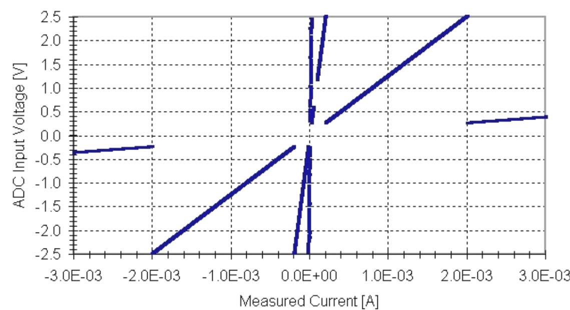


Fig. 6 – Zoom of Fig. 5 in the interval ± 0,2V.

Fig. 7 shows the input voltage of the ADC as a function of the current on the device under test, in the region where current scale changes. Notice that in the high resolution region the probability of stimulating ADC output codes is reduced due to the large increase in the voltage rate each time the current scale switches.



a)



b)

Fig. 7 – ADC input voltage as a function of the current on the device under test. b) Zoom a).

The excellent agreement between experimental and simulated data allows us to implement an error correction technique based on the numerical model here presented in order to increase the accuracy of the measurement results. The technique consists simply on the correction of the experimental voltage values by introducing the effect of different positive and negative gains and offsets. Doing this, the absolute error of the measurement calculated by (1) for a resistive load of 99,5 Ω is presented in Fig. 8. As one can see a great enhancement was achieved even near origin when comparing with Fig. 4. Further improvement on the model could theoretically be achieved by considering the effect of the system INL error in the region of high current scales. However the impossibility of synchronizing the theoretical and the experimental sampling times makes this infeasible.

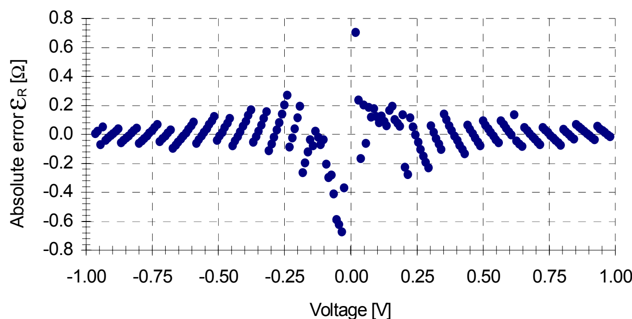


Fig. 8 – Absolute error of experimental measurements, after experimental voltage correction

IV. CONCLUSIONS

The numerical model presented in this paper was shown to be suitable to describe HP4140B behaviour. The model assumes that the main error sources are gain and offset errors. A least square algorithm was used to calculate gain and offset values from experimental data. Simulation results showed an excellent agreement with experimental measurement data. The absolute error between experimental and simulated I-V is similar to quantization error of a digitiser with magnitude within ± 0,5 LSB, despite origin.

By introducing positive and negative gain and offset error correction on experimental measurement data a great enhancement on resistance measurement was achieved, showing that this is an important tool to increase the accuracy of the instrument.

ACKNOWLEDGEMENTS

This work was sponsored by the Portuguese national research project reference POCTI/ESE/34424//2000, receiving a grant whose the authors gratefully acknowledge.

REFERENCES

[1] L. Angrisani, A. Baccigalupi, A. Pietrosanto, “A Digital Signal-Processing Instrument for Impedance Measurement”, IEEE Transactions on Instrumentation and Measurement, IM 45-6, pp. 930-934, Dec. 1996.

[2] M. A. Atmanand, K. Jagadeesh, V. G. K. Murti, “A Microcontroller Based Scheme for Measurement of L and C”, Measurement Science and Technology, Vol. 6, pp. 576-581, May 1995.

[3] M. Fonseca da Silva, A. Cruz Serra, "Study of the sensitivity in an automatic capacitance measurement system", IEEE Instrumentation and Measurement Technology Conference, IMTC/97 Proceedings, Vol. 1, pp. 329-334, Ottawa, Canada, May 1997.

[4] W. Yang, “A Self-Balancing Circuit to Measure Capacitance and Loss Conductance for Industrial Transducer Applications”, IEEE Transactions on Instrumentation and Measurement, IM 45-6, pp. 955-958, Dec. 1996.

[5] M. Fonseca da Silva, Pedro Ramos, A. Cruz Serra, "Impedance measurement using sine-fitting algorithms", accepted for publication in Measurement, Elsevier Science B. V., 2003. In press.

[6] P. Santos, A. Casimiro, M. Simas and M. Lança, “CMOS Compatible HV Gate-Shifted LDD-NMOS”, IEEE Trans. on Electron Devices, vol. 48, n. 5, pp. 1013-1015, May 2001.

[7] Hewlett Packard, “Model 4140B pA meter/DC voltage source – operation and service manual”, 1983.

[8] F. Correia Alegria, Pasquale Arpaia, Pasquale Daponte, A. Cruz Serra, "Performance analysis of an ADC histogram test using small triangular waves", IEEE Transa. on Instrumentation and Measurement, vol. 51, n. 4, pp. 723-729, August 2002.

Authors: Henrique Quaresma, António Pedro Silva and António Cruz Serra, IT/DEEC, IST, Universidade Técnica de Lisboa, Av. Rovisco Pais, 1049-001 Lisboa, Portugal, phone: +351-218418490, fax: +351-218418472, email: hjq@lx.it.pt, aprbsilva@hotmail.com, acserra@alfa.ist.utl.pt