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PROGRAMABLE SYSTEM FOR LOW FREQUENCY NOISE MEASUREMENTS IN MICROELECTRONICS DEVICES CONTACTED BY POINT PROBES

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Abstract − A novel system for low frequency noise, LFN, wafer-level (point probe) measurements and a method of the system calibration with the thermal noise of resistances are discussed. We also present some LFN data on MOSFETs as an example of implementing the LFN measurement technique for the device quality diagnostics.

Keywords: Noise measurements, MOSFET

1. INTRODUCTION

The signal to noise ratio is known to decrease with the device miniaturization. A continued reduction in their dimensions will inevitably necessitate taking measures towards the noise reduction. Studies of the LFN serve for the diagnostics of the field effect and bipolar transistors, MOSFETs and BJTs and provide indications for the device improvement. In the MOSFETs the power spectral density, PSD, of drain current, I_d, fluctuations is routinely used for evaluating the density of slow interface states, N_{st}, [1, 2], which we shall briefly describe here as an illustration of the operation of the programmable point probe noise measuring system, 3PNMS, that we present in this paper.

2. MEASUREMENT SET-UP

The renewed interest in the LFN measurements in transistors is linked with the equipment development (e.g. [3-5]). The 3PNMS [5-7] is, to our knowledge, the first LFN measurement system, which is both, fully programmable and immune to computer-generated electrical perturbations in the wafer-level (point probe) operation.

The system consists of a probe station, featuring four floating coaxial point probes, mounted on XYZ stages of micro-manipulators for device contacting, and the biasing and data acquisition electronics system (Fig. 1). The system's electronics is comprised of a (i) computer, equipped with an analogue-to-digital converter, ADC, card and a universal digital-lines output card, and (ii) computer-controlled current/voltage converter (I/V converter) whose inputs can be remotely biased (Fig. 2.) [5-7]. Henceforth we shall refer to the latter as a programmable biasing amplifier, PBA.

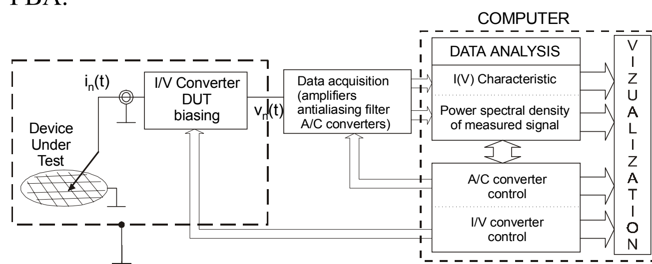

Fig. 1 Schematic diagram of the measurement set-up

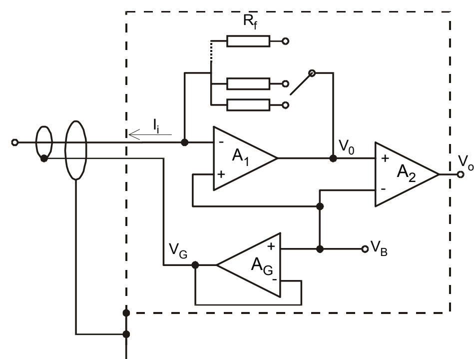

Fig. 2 Schematic diagram of the programmable biasing amplifier (PBA)

Fig. 2 presents the simplified version of the PBA, with a single input, for current measurements and DUT biasing. For the transistor characterization, a two-input version of the PBA was developed (PBA2). It features the biasing of two inputs, 1 and 2 (e.g. for drain and gate connections) and provides a current measurement in Input 1 alone [7]. The both inputs are triaxial, with guard potential applied to their inner shields (connected to the respective probe shells), in order to reduce the cable leakage and their effective capacity [8]. Input 2 provides V_g, with no current measured, whereas I_d, forced by the bias V_d, is measured in Input 1. The current amplifier gain, $G_{DC}=R_f$, is software-selected so as the optimal device-noise/system-noise ratio is maintained, with

V_{out} below the saturation value of the current amplifier. The proper R_f value is selected using bi-stable relays whose state is changed by digital signals, from a digital output PC card.

In the set-up the Cascade Microtech probes, installed on XYZ manipulators are used. In order to eliminate effects of external disturbances (such as mechanical shocks or EM interferences), the probe station is placed on the anti-vibration stone table and shielded. The shield ground and the system common are electrically separated. A considerable care has been taken to the cable layout in order to eliminate the ground loop effects.

The data is stored by a National Instrument DSA4452 card [9] plugged in the computer. The card has four analogue inputs, which serve for the alternative, AC, and direct, DC, current measurements for monitoring the biasing potentials applied to the terminals of the device under test (DUT). Each input channel of the DSA4452 is independently configured (e.g. its amplification, input range, the data acquisition parameters are all software-controlled).

The application for controlling the measurement set-up was developed using the National Instrument LabView environment. The application controls the biasing of the DUT, PBA's gain, data acquisition and analyzing, including results presentation and storage in text files.

The static characteristic measurement algorithm allows for a variation of one of the biasing voltages (V_b for BJTs and V_g for the FETs), leaving the bias on the second input constant (V_c and V_d respectively). The DUT current is measured for each biasing point on Input 1 of the PBA2. The software enables computer control/monitoring of only two values: one being the device bias voltage and the second the current flowing through Input 1 of PBA2. The static characteristic of the DUT is measured step-wise in a range of biasing voltages defined by the user. The measured characteristic is displayed in real-time on the application panel's graphical display. The noise measurement sub-application can be activated at each biasing point used for the static measurement.

The time-domain signal is digitized and then used for calculating a Fourier-transform (using a fast Fourier transform, FFT, algorithm). The averaged PSD function is subsequently presented in a sub-application graphic display and the PSD value at a selected frequency is returned and sent to the result array, together with respective static data. After finishing the measurement for a requested bias range, the result array is automatically stored in a text file. The single spectra for each biasing voltage can be also stored in a text file for a further processing.

When used in the automatic measuring mode, the system can store averaged PSD spectra of drain current fluctuations at drain current range $10^{-10}A<I_d<10^{-4}A$, with a default storage of PSD values S_{Id}, measured at an arbitrary selected frequency, f_0 (here 10Hz) in a text file, whose i-th line has the following format (V_{gi}, I_{di}, S_{Idi}, G_{dci}, V_d, f_0). The file can be further used for determining the interface density of defects responsible for the noise generation [1, 2]. The latter involves extracting from the data the 1/f noise component, by subtraction from S_{Idi} the appropriate PSD values measured at I_d=0. No operator's intervention is needed during the LFN measurements, but the monitoring of V_d, V_g, $I_d(V_g)$, and the spectra is provided in real time, via virtual instrument panels.

Several series of tests were performed in order to examine the systems reliability in noise measurements. The tests comprised both, static and noise measurements on the electronic elements, wire-bonded, and contacted on the wafer. In Fig. 3 we present some data for the PSD measurements taken on encapsulated and probe-contacted MOS devices, originating from identical wafers. The noise generation in the point probes proved to be negligible, as the results obtained on encapsulated devices matched those measured on their wafer-level counterparts.

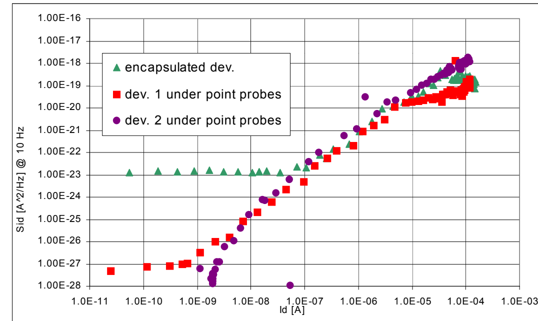

Fig. 3 The PSD of the drain current fluctuations *vs* drain current, I_d, taken on the wafer level (two transistors) and on an encapsulated device

The system was calibrated with thermal noise of resistors treated as reference. A schematic diagram of the calibration circuit is presented in Fig. 4.

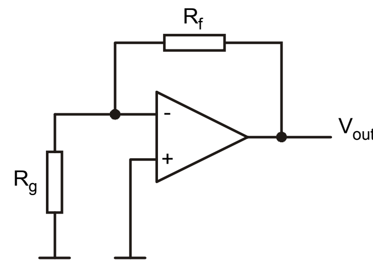

Fig. 4 The basic circuit diagram for calibrating the I/V converter with a thermal noise

Neglecting the inherent noise of the operational amplifier, the power spectral density of the input-referred current noise is [10,11]

$$S_{in} = 4kT\,(1/R_f + 1/R_g), \tag{1}$$

then the power spectral density of the output voltage is

$$S_{Vout} = 4kTR_f^2(1/R_f + 1/R_g). \tag{2}$$

The calibration method was verified experimentally by measurements of the output noise voltage for various values of R_g (10kΩ to 100MΩ) and R_f (10kΩ to 100MΩ). Fig. 5 shows the measured and calculated with (2) values for each pair of R_g and R_f. The analysis of the results allowed evaluating the influence of the system's inherent noise on the measurements.

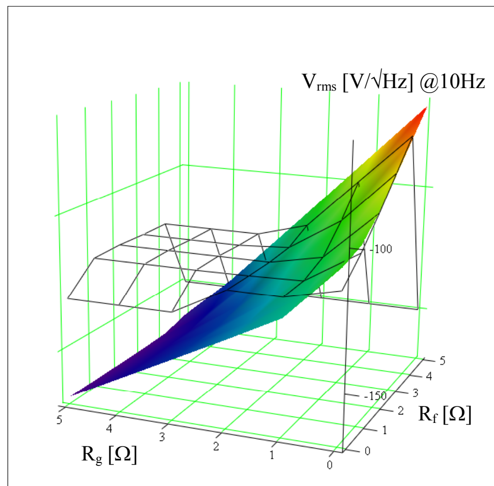

Fig. 5 The illustration of the system inherent noise influence on calibration with thermal noise. Surface - calculated values (Eq.(2)), mesh - experimental results for R_f (10^3 Ω to 10^8 Ω) on X axis and R_g (10^8 Ω to 10^3 Ω) on Y axis

It was experimentally established that the inherent noise influence on calibration results is lower than 5% for all values od R_f for 100MΩ>Rg>10MΩ.

3. EXPERIMENTAL RESULTS AND DISCUSSION

The test devices were fabricated using a standard 50nm nMOSFETs process. The description and characteristics of the devices have been presented elsewhere (see [12,13] and references therein).

Using the 3PNMS the static and noise measurement were taken on devices for the drain current range from 10^{-10}A to 10^{-4}A at V_d=50mV. Using the FFT algorithm, the power spectral density, PSD of the I_d fluctuations was calculated and its value for frequency f=10Hz was stored with corresponding I_d and gate voltage, V_g values for further processing. Fig. 6 shows the PSD of I_d fluctuations for four thin gate oxide MOSFETs of the same type. As it can be seen, the reproducibility of the results is satisfactory.

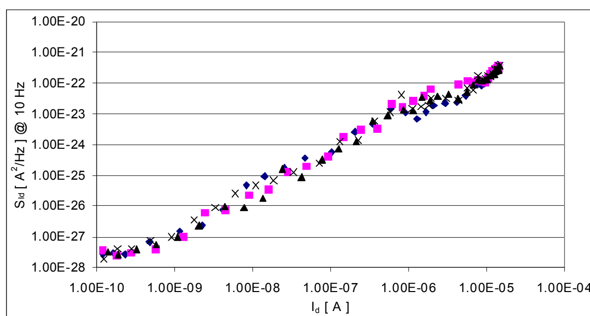

Fig. 6 The power spectral density, S_{Id} of the I_d fluctuations as a function of the I_d; devices t_{ox}=25Å, W=L=10µm

The S_{Id} can be expressed as [1,2],

$$\frac{S_{Id}}{I_d^{\,2}} = \left(\frac{S_{Id}}{I_d^{\,2}}\right)_{\Delta\mu} + \left(\frac{S_{Id}}{I_d^{\,2}}\right)_{\Delta n} + \left(\frac{S_{Id}}{I_d^{\,2}}\right)_{\Delta Ra} . \quad (2)$$

The first term in (2) represents the noise resulting from mobility fluctuation

$$\left(\frac{S_{Id}}{I_d^{\,2}}\right)_{\Delta\mu} = \frac{q\alpha_H}{WLQ_i f} , \quad (3)$$

where f is the frequency, α_H is a Hooge parameter and Q_i is the inversion charge[2,14].

The second term in (2) represents the carrier number fluctuation, Δn noise. This component originates from the fluctuations in the total number of carriers in the channel and is defined as,

$$\left(\frac{S_{Id}}{I_d^{\,2}}\right)_{\Delta n} = S_{vfbn}\left[1+\alpha_c C_{ox}\mu_{eff}\frac{I_d}{g_m}\right]\left(\frac{g_m}{I_d}\right)^2 , \quad (4)$$

where α_c is a coefficient measuring the correlated Δn-Δµ noise, C_{ox} is the electric capacity of the gate-drain capacitor, μ_{eff} is the effective mobility, $g_m=\partial I_d/\partial V_g$ is the transconductance, obtained from an independent static measurement and S_{vfbn} represents the flat band potential fluctuations,

$$S_{vfbn} = \frac{kTq^2 N_{st}}{WLC_{ox}^{\,2} f} , \quad (5)$$

where N_{st} (in $cm^{-2}eV^{-1}$ units) is a surface density, per unit energy, of slow trap centers assumed to be localized near the $Si\text{-}SiO_2$ interface.

Finally, the last term in (2) represents the noise generated by the access resistance fluctuations.

$$\left(\frac{S_{Id}}{I_d^{\,2}}\right)_{\Delta Ra} = S_{Ra}\left(\frac{I_d}{V_d}\right)^2 \quad (6)$$

The contribution of each component of (2) into the total noise of the device depends on the I_d range. For low currents the Δµ component dominates. In a middle-value current range the dominant is Δn component, while for high current (I_d values close to saturation) the contribution of the access resistance is considerable.

Using (2) the power spectral density of the 1/f noise normalized by I_d^2 was calculated. Several parameters needed for the calculation were extracted from the static measurement data. Subsequently the calculated data were compared with those obtained from the measurements. Some results of the calculation and the measurements are compared in Fig. 7.

The solid line presents the best fit of the the calculated values to the data. The data for $I_d>10^{-8}$A can be accounted for by (4) and (5) with $N_{st} \approx 10^9/cm^2eV$. This value is typical for good-quality Si/SiO_2 interfaces.

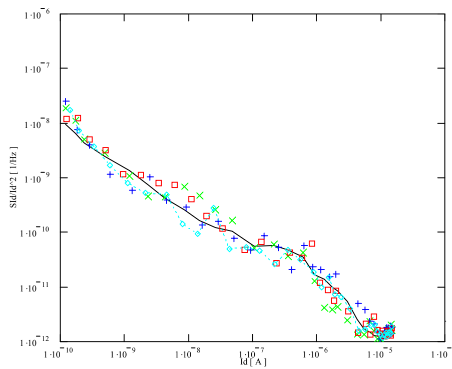

Fig. 7 Measurement (points) and simulation (line) data obtained on a MOSFET with L=W=10µm and 25Å -thick gate oxide

3. CONCLUSIONS

In this paper we presented a novel computer-controlled, fully programmable system adapted for wafer-level, point probe LFN measurements. The system enables automatic measurements of static and noise characteristics of the microelectronics devices. The tests performed on various devices showed that the implementation of the point probes does not decrease the reliability of measurements.

We have demonstrated that a computer-controlled, fully programmable system for LFN measurements on a wafer–level can be successfully used for the device characterization with the LFN measurement techniques. In the MOSFETs, the trap density can be extracted from the data in terms of the existing model [1,2] of the LFN generation. The automation of the measurements enables repetitive transistor testing, providing a non-destructive, wafer-level method for the interface trap density evaluation in the MOSFETs.

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