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DESIGN-FOR-TESTABILITY IN EMBEDDED MEASUREMENT SYSTEMS

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Abstract – Test and self-diagnosis are important for the reliability of embedded measurement systems. For such mixed-signal systems it was introduced any special methods of design-for-testability. This paper will discuss any problems of possible structures by using the analogue Boundary-Scan method and its implementation.

Keywords: design-for-testability, analogue Boundary-Scan, embedded mixed-signal systems.

1. INTRODUCTION

Measurement systems include a lot of analogue and digital elements with different but increasing complexity. All elements are coupled in the electrical circuit to realise the wanted function. The increasing grade of integration brings out great problems for production tests, because of the extreme decreasing possibility to access all of the internal nodes. But, the node access is the basic condition for any ability of controlling and observation the unit under test. Therefore a new method of design-for-testability was innovated in 1991 with the standard of Boundary-Scan [1], at first for digital circuits.

The principle of Boundary-Scan is, to include an additional test structure, which bound the electronic circuit, which has to be test. The approached test structure consists of digital boundary modules (DBM), implemented in all functional digital pins of the integrated circuits, which are connected to a shift register, the Boundary-Scan register. Every scan-able circuit include a test access controller port (TAP), which is controlled over the test bus signals. This technology can be very successful in pure digital systems.

The problem by using this successful method in measurement systems is driven by the high quantity of analogue elements in the interface to the mainly analogue world. In the most cases this problem is solved by using additionally test methods, like in-circuit or visual tests. But, this is only a way in the area of the production test.

The increasing large integration of analogue circuits and the smaller dimensions of these elements exclude this practice more and more. This task is additionally complicated for the field of self-diagnostics. In this area with smallest dimensions it is not possible to use any external probes to contact interesting internal nodes. So it was necessary to introduce a new method for testing connections in the analogue area. The technology of analogue Boundary-Scan was created [2][3].

2. USING ANALOGUE BOUNDARY-SCAN IN EMBEDDED SYSTEMS

2.1. Basics of analogue Boundary-Scan

The basic structure of the analogue Boundary-Scan test bus is shown in **fig. 1**. Similar to the digital test bus (IEEE1149.1) with DBMs in all digital functional pins, there are implemented analogue boundary-scan modules (ABM) for all analogue functional pins. This standard use the same digital scan chain to control the test structure – and so it can drive analogue scan tests and digital scan tests too. Additional analogue test busses are implemented for driving and sensing of analogue test signals controlled by an analogue test bus interface circuit (TBIC).

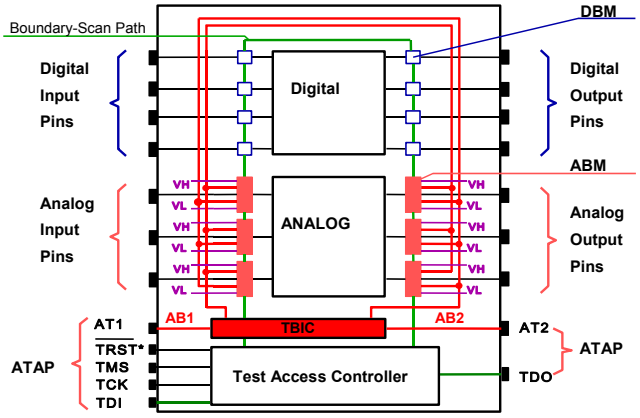

Fig. 1: Circuitry with IEEE1149.4

The principle of such an ABM-cell is shown in **fig. 2**. With that standard test structure it is possible, to observe one functional net on the board and - also - to drive a signal into one net - without any mechanical probes. Only the connections for the digital and analogue test bus lines are necessary for testing (- and of course the digital test bus).

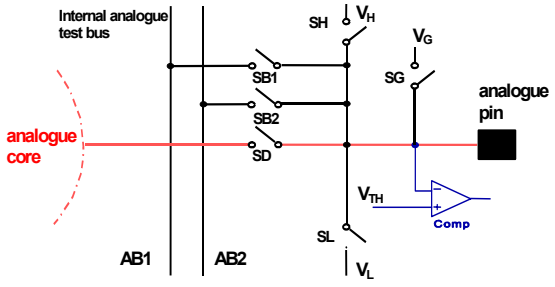

Fig. 2: Principle of an ABM cell in an IEEE1149.4 IC

2.2. Practical problems and steps for solving

A successful application of such a test structure needs the following of special rules for design of the system and its implementation. Problems, which have to be discussed and solved, are the following

1. Choosing of suitable boundary-scan-able circuits for an implementation of the wanted function
2. Basically design of testable structures in the aimed system by partitioning in areas of similar elements (analogue / digital, scan-able / non-scan-able, static / dynamic tests and so on) and design of the corresponding test structure
3. Proofing of any resulting interference for the wanted "normal" function, especially in the analogue area
4. Design and verification of functional circuits and test elements, including test steps
5. Optimisation of test structure, test steps and test sequence (long scan chain, special test conditions)
6. Proofing of undefined conditions for tests, switching mode, initialisation, undefined or critical test respectively functional parameters

It is essential for best results, that the designer has to consider the rules of design-for-testability from beginning of the design process.

Of course, in this time there are a lot of problems in these presented fields, because of the non-availability of different certified scan-able analogue components (for the first point). Therefore it is wide more important, to disregard especially point two, the structural partitioning and design-for-testability. In the principle the designer has to disregard the same known rules from digital scan-able systems and especially of course the DFT-rules from the in-circuit test in mixed-signal systems. By means of the following example circuit are discussed any possibilities.

2.3. Example

Figure 3 shows an example for an analogue input circuit with simple possibilities for analogue data processing and self-calibration, using an industrial analogue scan-able multiplexor circuit with two 2-1-multiplexor functions [4].

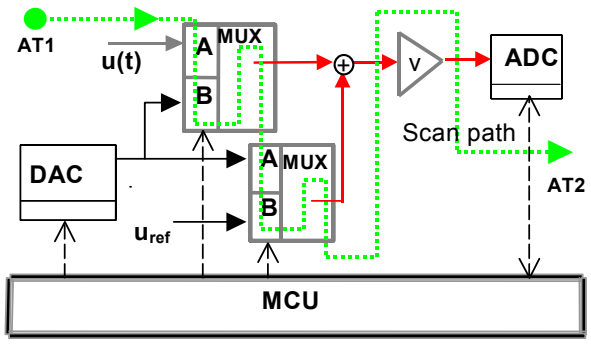

Fig. 3: Principle of self-calibrating input circuit

The discussed unit was chosen, because of it can be a model both for a self-calibrating input circuit and an embedded high-integrated system with usually reduced testability. Special new solutions are required here. The strategy of design-for-testability can be one way for a cost-effective solution of these problems.

The mostly aimed feature of this unit is the "normal" function of an input circuit of a measurement input channel with high qualified and stable properties. This can be reached by using of special calibrated components (like reference elements) in a structure with feedback. The calibration has to be implemented by a cyclic task, but without any external devices.

First step is to test the analogue digital converter (ADC) for fixed values of reference voltage by activation of the reference digital analogue converter (DAC). The micro-controller unit (MCU) stores the results and calculates the offset error and the gain error. With these measured reference and correction values the MCU corrects the ADC values of the measured signal u(t). Proposed the characteristic of the realized analogue channel is very good linear, it is used a simple linear correction function. The stored offset error serves for an active offset compensation by hardware. This board can be driven in different modes. In the following part will be discussed any results of first measurements.

2.4. Measurements

Figure 4 shows the measured DC-error over this scan-able multiplexor. The resulting error is very small in the voltage area – smaller than 2,5 V - and can be neglected. The apprehended influence of such an analogue test structure is not really significant (**Fig. 5**). That means, that the reserve of developers is not really justified with looking at the technical feasibility.

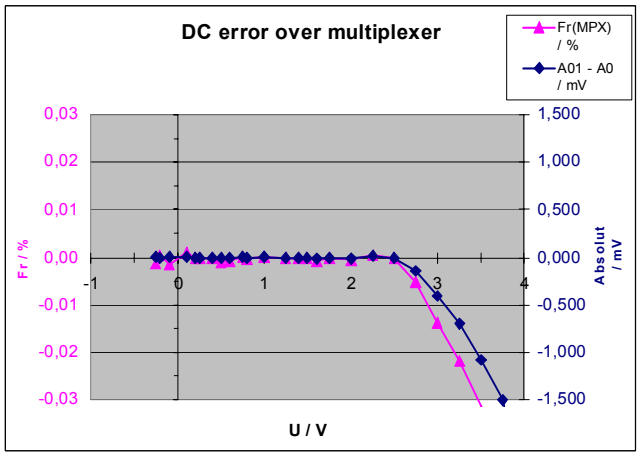

Fig. 4: Measured DC-error over multiplexor IEEE1149.4 IC

But the measurement result over all shows, that there is a significant amount of the gain error and the offset error, caused from the amplifier unit (**fig. 6**). In this example the gain error can reach up to four bits, if it is used a resolution of 16 bits. To keep the maximal working range, it is implemented an active mode for correction of the offset error. The MCU have to realize the following steps, only one times in the calibration step:

1. Measuring the offset error
2. Calculate the correction voltage u_{kDAC}
3. Set the DAC to u_{kDAC}

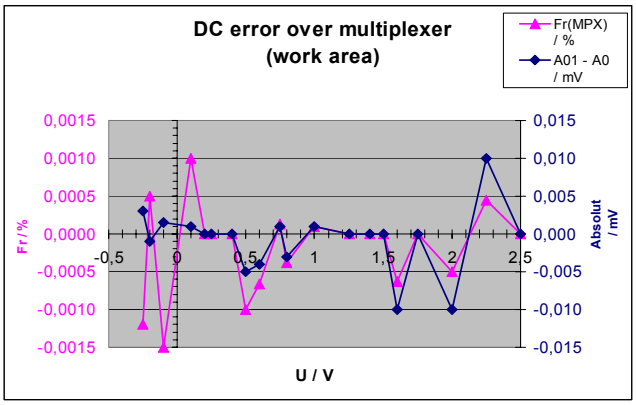

Fig. 5: Measured DC-error over multiplexor IEEE1149.4 IC (Detail for higher resolution)

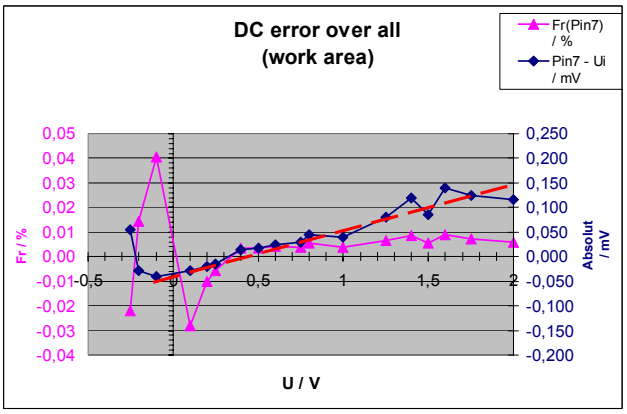

Fig. 6: Measured DC-error over all (multiplexor and operational amplifier circuit)

The gain error correction can be realized from the MCU by special algorithm with the following steps:

1. Measuring the transfer function with any voltage steps (DAC) by using of
   - Additional/special multiplexor circuit and a reference voltage from the reference block or
   - An included test structure, corresponding to the standard IEEE1149.4 (by using of the standard instruction PROBE)
2. Calculate the parameters of the correction function
3. Use the calculated correction function (from step 2) in every sampling cycle.

Steps one and two have to be done only once in the calibration step. By doing these steps, it will be possible to get the real measurement values and to use the high resolution over the whole voltage range. The time distance between two calibration cycles has to define in dependence on the requirements for precision and availability of the function and from its reached stability.

2.5. Design-for-testability in an analogue system

The strategy of design-for-testability (DFT) is not only important for the field of production tests. Especially for an embedded system it is necessary, to implement possibilities for self-testing and self-calibration. Both tasks need the comparison of measured results with expected values, driven from known signal sources with reference quality.

For more complex systems it will be the first task, to divide the network in testable parts. This is solved for digital systems by controlled enable-lines of bus or output drivers. In some cases it is necessary to implement additionally controllable driver circuits for the partitioning of the system. The testability can be increased, if such additional driver circuit is scan-able. Then this circuit gives moreover the possibility to access to the internal nodes of the system with virtual needles. This practice is also useable in an analogue system, of course.

In **figure 7** is shown the principle of partitioning with scan-able mixed-signal circuits in the analogue part of the system by using the available IEEE 1149.4 analogue test access device. The picture demonstrates the possibility, to divide a complex system in smaller parts, which are easier for testing and diagnosis. This structure gives the possibility to inject a reference signal into the following isolated network. In the most cases there are anyway implemented drivers between functional units for decoupling and adapting different impedances. Now, these IEEE1149.4 circuits are used like buffers. They offer additional features by the implemented and standardized analogue boundary scan modules.

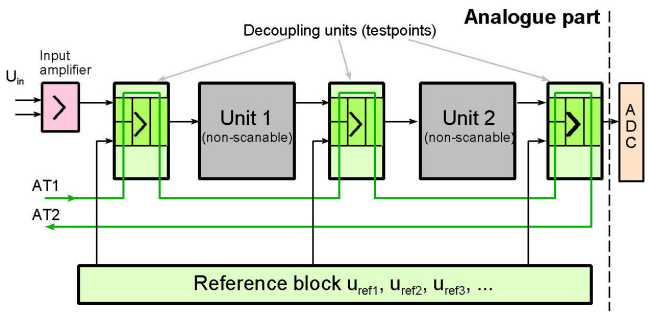

Fig. 7: Principle of partitioning with scan-able circuit in the analogue part of the system

The multiplexor circuits are used to isolate the different functional units. With these multiplexors the on-board control unit (here not-shown) can switch between the "normal" signal and a reference signal source. This can be done one after the other for all separated units, also for the complete chain.

The same possibility is given by employing of the IEEE1149.4 test structure by using the instruction PROBE. With this instruction the control unit can force the injection of a reference signal over the analogue test bus line AT1 into one internal node at one time. The answer oft his stimulation can be proofed by measuring of the resulting voltage values on every of the scan-able internal nodes. So it is also possible to test the transfer function between several nodes. To guarantee defined test conditions respectively stable state of any free running part on the board, other nodes can be driven from separately reference sources, selected by switching of the multiplexors, or driven from its ABM-internal reference sources of the standard test

structure (v_H, v_L or v_G in fig. 2). The principle of such a measurement and simple examples was shown in [5].

Of course, a lot of problems occur in the analogue area by using of non-ideal elements. A practicable IEEE1149.4 buffer/driver circuit has to be developed specifically for the concrete application field, which has to be described especially by voltage and frequency area. The input and output parameters are also very important. These problems are any more difficult like in the digital world. Therefore the better way will be to include the test structure directly in the functional circuits. Then the input and output drivers adapt the functional unit internal on the basis of the same semiconductor technology. The test structure and the functional most important elements can be optimised for the aimed function and for significant parameters of the whole circuit.

If the boundary scan test structure is implemented in a system, then should it be useable for self-test too. This is very important especially, if the system should work like a separate installed embedded system and if a high reliability is required. Moreover, it is realizable also in mixed-signal systems.

A structure of a self-testing unit in an embedded mixed-signal system is given in **fig. 8**. The digital test structure IEEE1149.1 needs an additional multiplexor unit for different test modes:

1. Production test mode in the production test field
2. Self-test mode in the application field.

For the production test mode the test bus is connected with the external boundary-scan tester. In the self-test mode the embedded MCU drives directly or by controlling of a special boundary-scan master unit the test bus. Additionally, the analogue test bus line AT1 is driven by a DAC over a controllable output amplifier, which can drive an adjustable current. The resulting voltage level on the analogue test bus line AT2 has to be measured by ADC, driven by an adjustable input amplifier.

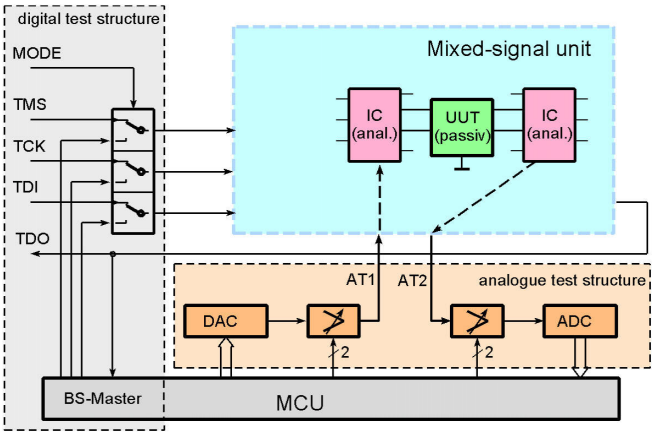

Fig. 8: Structure of the self-testing unit in an embedded mixed-signal system

The most important request to the analogue source is to guarantee reference quality in the aimed temperature area over long time, not resolution or speed. The adjustable amplifier has to adapt the amount of output current to the range of the parameter, which to be test. Its output needs a voltage protection against too high resulting voltage levels. For the measurement input the resolution is most important. This can include a low pass filter to minimize the noise influence.

Such a structure can realize self-testing of internal DC levels, transfer functions between any internal nodes, electrical connections and parameters of important functional elements or nets. The feature of self-test ability is very interesting for the field diagnosis, including on-line far distant diagnosis about a wide area network. Most of the additional required elements to realize such a structure are included in modern standard controller units or programmable in a standard FPGA, so that the total count of elements must not increase significantly.

3. CONCLUSIONS

It is shown, that it is possible to design a measurement system with integrated analogue test structure without to impair the important aimed parameters significantly. There are new requirements for using a DFT-strategy, but there are also new DFT possibilities for analogue systems by using the standard IEEE1149.4. If the test structure is implemented in standard components, similar to the digital boundary-scan components, then the additional costs are not really important.

Therefore it is necessary to force the developing of analogue scan-able circuits and corresponding test systems. Then it will be possible to increase the testability of mixed-signal boards and - at all - to reduce the test costs. Additionally, it will be possible too, to implement new features for self-testing and self-diagnostics to get embedded measurement systems with higher reliability.

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