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Phase Noise Measurement of ASIC Voltage Controlled Oscillator and PLL Circuit ADF4002

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* ***Abstract –*** **This article describes phase noise measurement of a designed ASIC voltage-controlled oscillator in 0.25 µm SiGe BiCMOS technology, with frequency synthesizer ADF4002 from Analog Devices. The oscillator topology utilized in this design is based on a crosscoupled-transistor configuration, and it incorporates two options for frequency control: varicap and capacitor bank. The oscillator frequency is 11.13 GHz with an adjustment frequency range around ±250 MHz. Phase noise measurements were performed on a custom evaluation board. Oscillator with PLL achieves phase noise λ(100 kHz)= -70 dBc at f_c = 11.1353 GHz. The article contains phase noise measurement of ASIC comparisons based on selected parameters, dividers and ADF4002 settings. Comparison with the commercial oscillator TGV2566SM and PLL ADF4002 is introduces as well. Details of the measurement setup and different filter parameters are discussed.**

I. INTRODUCTION

Phase noise measurement is a critical aspect in the characterization and evaluation of voltage-controlled oscillators (VCOs) used in modern communication systems. VCOs are essential components in frequency synthesizers, which are widely used in various applications such as wireless communication, radar systems and satellite communication. The accurate measurement of phase noise helps determine the stability and spectral purity of VCOs, thereby influencing the overall performance of these systems.

We are currently concentrating our research efforts on the creation of a sensor system using Ultra-Wideband (UWB) M-sequence technology. This UWB system has various applications such [1],[2],[3]. Throughout our work, we have successfully designed several specialized rf circuits including a mixer [4], Ultra-wideband amplifier [5], divider [6], and UWB transceiver [7].

In this article, we delve into the phase noise measurement of a designed ASIC VCO implemented in a 0.25 μm SiGe BiCMOS technology by IHP. The VCO is assembled on an evaluation board with the Phase locked loop circuit(PLL) ADF4002 from Analog Devices, which offers enhanced frequency control capabilities. The oscillator topology utilized in this design is based on a crosscoupled-transistor configuration, and it incorporates two options for frequency control: varicap and capacitor bank. This dual control mechanism allows for precise adjustment of the VCO frequency within a range of ±250 MHz around the central frequency of 11.13 GHz.

To evaluate the characteristics of the designed VCO, we performed phase noise measurements on a custom evaluation board. When coupled the VCO with a phase-locked loop (PLL), phase noise level of λ(100 kHz) = -70 dBc/Hz at a carrier frequency of 11.1353 GHz was achieved. The article presents a comprehensive analysis of the phase noise measurements, focusing on various parameters such as dividers and ADF4002 settings [8]. By comparing the phase noise performance under different configurations, we gain insights into the effects of these parameters on the spectral purity of the VCO. Throughout the article, we

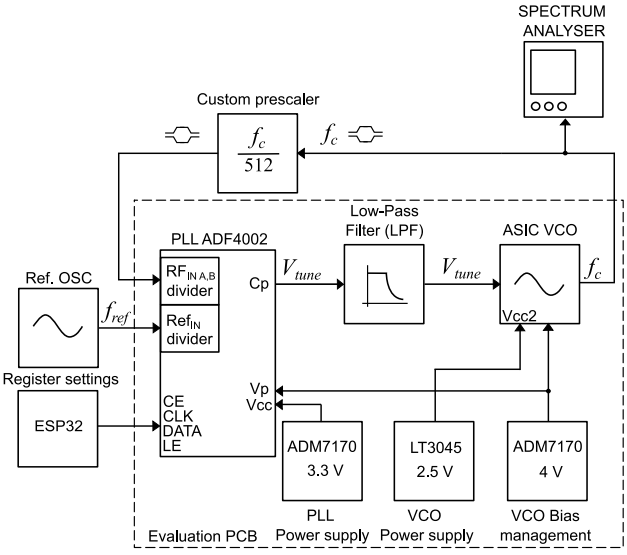

Fig. 1. Block diagram of single channel phase noise test set.

provide detailed information about the experimental setup used for the phase noise measurements. By elucidating the methodology used in this study, we aim to facilitate a thorough understanding of the phase noise measurement process for VCOs. The results and findings presented in

this article contribute to the advancement of VCO design and optimization, particularly in the context of frequency synthesizers for ultrawideband radar systems.

In section II. equipment setup and evaluation of printed circuit board will be discussed, in section III. voltage-controlled oscillator is discussed. Section IV. consist of measurement PLL+VCO configuration with filter variations and divider options. In summary, this article focuses on the phase noise measurement of an ASIC VCO implemented in a SiGE BiCMOS technology, utilizing the ADF4002 frequency synthesizer from Analog Devices. Through detailed experimental analysis, we examine the impact of various parameters on the phase noise performance, offering valuable insights for the design and evaluation of VCOs in modern communication systems.

II. EQUIPMENT SETUP AND EVALUATION BOARD

In Fig. 1 is a block diagram of the measurement setup and evaluation board. For measurement of phase noise was used an Agilent N9020A spectrum analyzer with a frequency range of up to 26.5 GHz. A Keysight N5183B signal generator with frequency range from 9 kHz up to 32 GHz was used as a reference oscillator (in Fig. 1 Ref. OSC). The evaluation board (Fig. 2) consist of Phase locked loop circuit ADF4002 with low noise power supply ADM7170 set to 3.3 V. The ADF4002 supports the ability to set internal circuit parameters using an SPI compatible bus [8]. We used the ESP32 development board to set the parameters of the reference oscillator divider(Ref_{IN}), RF signal divider(RF_{IN}), and other settings. The f_c signal fed to the ADF4002 is divided by 512 in the external divider since the ADF4002 operates in the range of 5 MHz to 400 MHz. The *Cp* output of the ADF4002 represents the V_{tune} voltage which passes through the low-pass filter block and is then fed to the varicap in the voltage-controlled oscillator. The oscillator is powered with ultra low noise linear regulator LT3045 with output set to 2.5 V. Designed ASIC VCO is possible to connect to external bias voltages to change DC operating point of internal circuits. For easier adjustment of these voltages, there are adjustment trimmers on the printed circuit board. As printed circuit board (PCB), the Rogers RO4360G2 material, with 0.508 mm thickness and $\varepsilon_r = 6.15$ was used. The whole evaluation board is powered by 5 V with 80 mA consumption. Our spectral analyzer does not contain an application for measuring the phase noise, based on that phase noise measurement where performed on a spectral analyzer with direct spectrum technique [9].

III. VOLTAGE-CONTROLLED OSCILLATOR DESIGN

Designed voltage-controlled oscillator is a differential oscillator based on BJT NPN transistors in crosscoupled

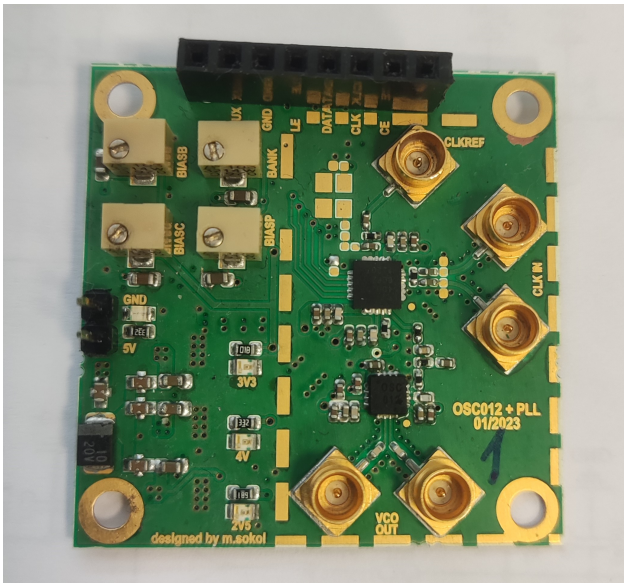

Fig. 2. Evaluation printed circuit board, substrate RO4360G2.

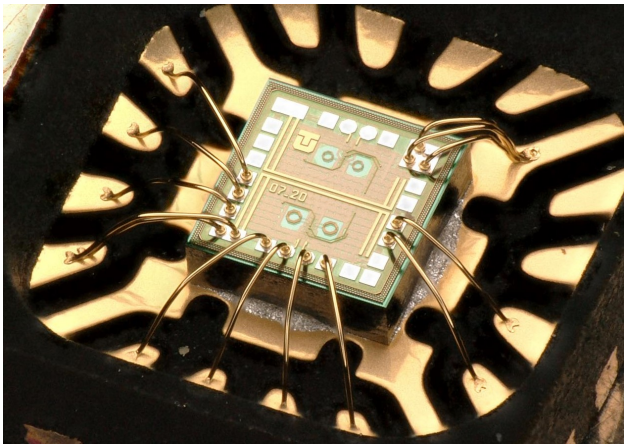

Fig. 3. Naked die of ASIC voltage controlled oscillator in QFN 3x3 mm package.

configuration topology, realized as an application-specific integrated circuit (ASIC)[10],[11],[12]. Fig. 3 shows a naked die, wire bonded in QFN package. The oscillator was primarily designed for the UWB sensor system operating in baseband, with master clock 11 GHz, and useful bandwidth up to 5.5 GHz. As mentioned the oscillator can be adjusted using 5 different bias voltages, three voltages are used to set the operating points of the transistors, and the remaining two are used for frequency control. Frequency of the oscillator can be controlled in two ways, by connecting the voltage to the varicap or by switching on the capacitive bank. For measurement described in this article the voltage on the varicap was regulated and voltage of the capacitive bank was set to a 0 V. The main advantage

of our custom oscillator is its low power consumption, the oscillator consumes only 40 mA at 2.5 V supply voltage. The oscillator itself is an unlocked free-running oscillator and does not achieve the required frequency stability, when locked to a PLL ADF4002 achieves better characteristics.

Component	Filter 1	Filter 2	Filter 3
C1	22 nF	100 pF	1 nF
C2	47 nF	4.7 nF	10 nF
C3	1.5 nF	100 pF	1 nF
R1	220Ω	1 kΩ	1 kΩ
R2	1 kΩ	1 kΩ	1 kΩ
Loop BW [kHz]	82 $\phi 30°$	456 $\phi 46°$	176 $\phi 350°$

Table 1. Filter component configuration.

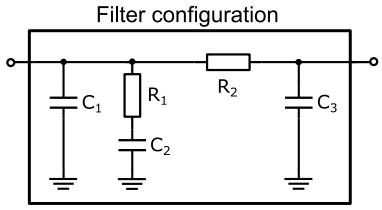

Fig. 4. Schematic of filter configuration.

IV. MEASUREMENT OF PLL+VCO

One of the key parts of the PLL and oscillator connection is the low pass filter applied to the V_{tune} voltage that drives the varicap. Analog devices provide a tool to simulate the effect of the filter ADIsimPLL [13].The low pass filter schematic is shown in Fig. 4. In article three filter configurations were tested with different component values shown in Table 1. The goal was to stabilise the oscillator frequency and suppress spurs around the oscillating frequency, and test the ADF4002 settings and compatibility with our ASIC. The reference clock(RF_{IN}) from external signal generator for ADF4002 was 42.540 MHz.

A. *Filter comparison with Divider Ref_{IN}/4 and RF_{IN}/2*

Fig. 5 shows a comparison of 3 filters, it is possible to see spurs around oscillating frequency. 3rd filter has a higher phase noise around 100 kHz from oscillating frequency, it is also possible to see higher spurs than filter options 1 and 2. Filters 2 and 3 exhibit better phase noise characteristics, and lower spurs. The divider in ADF4002 was set to divide reference frequency(Ref_{IN}) by 4. Divider for f_c frequency (RF_{IN}) was set to 2 for signal dividing. The max amplitude of all 3 configurations were -6.65 [dBm], and phase noise amplitude from oscillator frequency at 100 kHz was -70 dBc/Hz.

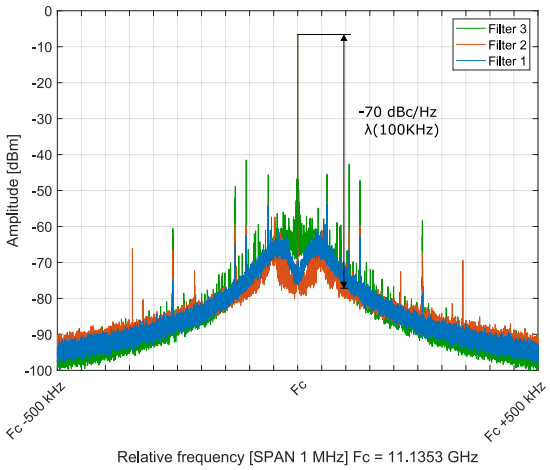

Fig. 5. Phase noise comparison based on used filters and set dividers of reference Clock (Ref_{IN}/4), and divider of oscillator signal (RF_{IN}/2), SPAN 1 MHz.

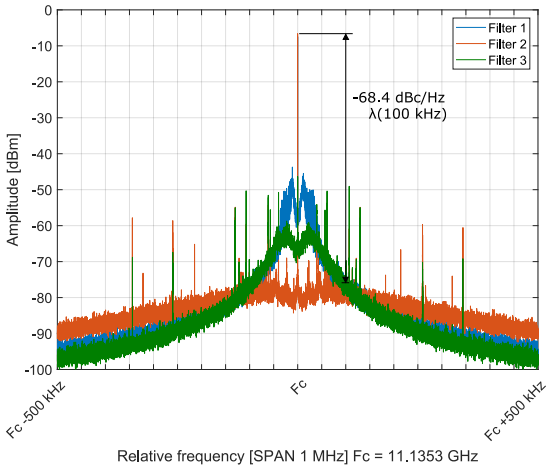

Fig. 6. Phase noise comparison based on used filters and set dividers of reference Clock (Ref_{IN}/2), and divider of oscillator signal (RF_{IN}/1), SPAN 1 MHz.

B. *Filter comparison with Divider Ref_{IN}/2 and RF_{IN}/1*

Different settings of ADF4002 were used in the second measurement, the reference clock divider was set to divide by 2 and divider of oscillator frequency f_c was set to divide by 1. This settings occurs on some occasion better performance. For a filter, configuration is possible to see from Fig. 6, the 2nd filter has the best phase noise characteristic -68 dBc/Hz at 100 kHz, but higher spurs occur around f_c. Filter 1 have the worst phase noise around oscillating frequency -45 dBc/Hz at 10 kHz but has a better tendency to decrease than filter 2.

C. Comparison of designed VCO+PLL and commercial VCO+PLL

We had a commercial voltage-controlled oscillator TGV2566SM [14] in connection with phase-locked loop circuit ADF4002 from Analog devices. This configuration is used in the UWB sensor node. To compare the phase noise envelope, we created a plot with the relative X-axis (see Fig. 7), the commercial oscillator operates at a different frequency (13.3119 GHz) than our oscillator (11.1353 GHz). From the graph, we can see the overall lower phase noise, In the vicinity of f_c is about -10 dBc/Hz and at the level of $\pm$ 500 kHz is about -15 dBc/Hz. Additionally, the graph also reveals the presence of lateral spurs at a level of around +-480 kHz.

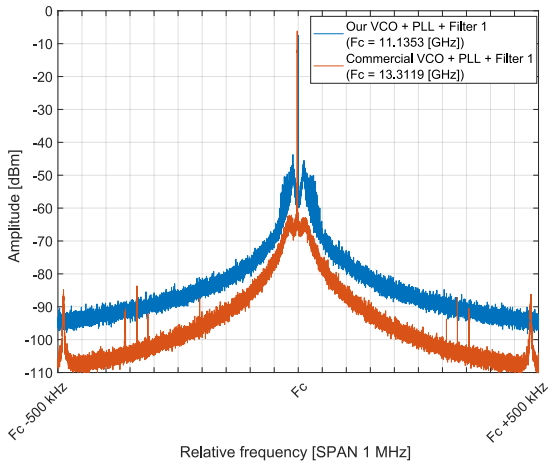

Fig. 7. Phase noise comparison of our solution and commercial solution, both solutions had filter configuration 1, $Ref_{IN}/2$ and $RF_{IN}/1$. Commercial VCO has different oscillator frequency (13.3199 GHz), because of that x-axis is relative for comparison.

V. CONCLUSION

This article presents an assessment board for an ASIC voltage-controlled oscillator that was designed in connection with the phase-locked loop (PLL) circuit ADF4002 from analog devices. The entire power consumption of the PCB was 400 mW, powered by a 5 V supply. The characteristics of the oscillator, in conjunction with the PLL circuit, were notably enhanced, particularly in terms of the stability of the output frequency at 11.1353 GHz and the overall phase noise. Among the three available filter configurations, configurations 1 and 2 are suitable depending on the divider setting of ADF4002. The oscillator achieved a phase noise level of -70 dBc/Hz at 100 kHz, with an output power of -6.65 dBm. Note that it is also important to take into account the losses that occur in the coaxial cables.

VI. ACKNOWLEDGMENT

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