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ADC Input Currents Measurement

Jakub Svatos[1], Jan Fischer[1], Jan Holub[1]

[1] *Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Measurement, Technicka 2, 166 27, Prague 6, Czechia, svatoja1@fel.cvut.cz*

***Abstract* – The contribution introduces the possible issue of internal CMOS Successive Approximation Register microcontroller's Analog-to-Digital Converters input currents. If the microcontroller also contains a multiplexer, it can lead to consequences caused by the sample-and-hold block that is part of a charge redistribution Analog-to-Digital Converter. The article presents its nature, the possibility of its measurement, and a simplified model of such an MCU analog inputs behavior. The simplified model and derived formulas can help the unacquainted user in a data acquisition system with the MCU design when measuring signal sources with non-negligible internal resistance. The introduced parameters, which cannot be found in datasheets, can be essential for users.**

I. INTRODUCTION

Current microcontrollers (MCU) very often contain one or more CMOS Analog-to-Digital Converters (ADC) working on the Successive Approximation Register (SAR) principle with a typical resolution of 12 bits [1]. These MCUs are usually also equipped with a multiplexer. By the nature of the CMOS ADC principle, it inherently contains a sample-and-hold (S/H) block [2]. However, this S/H block is not independent, but it is part of the charge redistribution ADC, which results in differences from the classic S/H and, therefore, consequences that unacquainted users may not expect. The fundamental difference lies in the fact that the charge on the sampling capacitor in the CMOS ADC changes during the process of SAR operation. Each time a new sample is acquired, the measured circuit is loaded with a current pulse. This is a typical feature of CMOS SAR ADC used in MCU, which, with some exceptions (ATmega328), usually does not contain an analog buffer. In the case of specialized ADCs [3], an auxiliary block, "precharge," is used, which reduces the load by precharging the sampling capacitor to a charge corresponding to the previous sample [4]. However, this is not the case with the ADC used in MCUs. Therefore, in this type of ADC, it is necessary to take into account the current pulses in the sampling processor. These parameters are not presented in the datasheets of the manufacturers [5] and [6].

II. S/H BLOCK IN CMOS SAR ADC

The task of a classic S/H block based on bipolar technology is to maintain a constant voltage at its output during the entire conversion process of the ADC. The situation is shown in Fig. 1. The sampling capacitor is followed by a buffer with a large input impedance driving an input of the ADC [7].

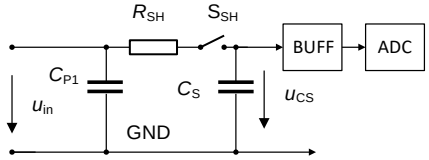

Fig. 1. Classic S/H block use with an ADC.

The input voltage u_{in} is applied to the passive S/H circuit, which takes a new sample $u_{in}(n)$. During the sampling, a transient response occurs when the voltage on the sampling capacitor C_S according to Fig. 1, must change from the previous value of $u_{in}(n\text{-}1)$ to the new value of $u_{in}(n)$. When simplifying and neglecting the capacitive charge feedthrough from the control circuit, a charge ΔQ_S flows through the S/H switch, proportional to the voltage change between the two samples.

$$\Delta Q_S = (u_{\mathrm{in}}(n) - u_{\mathrm{in}}(n-1))C_s \qquad (1)$$

If a constant input voltage u_{in} is sampled, the voltage u_{CS} on the hold capacitor practically does not change. Therefore, the capacitor does not need to be charged or discharged again, and no current flows through the input. This is entirely different from a conventional CMOS SAR ADC. During the charge redistribution process that takes place in the CMOS ADC, the voltage on the capacitor C_S, which is part of the ADC, changes. With each new sampling, even from a source of constant voltage, C_S must always be recharged to a value corresponding to the measured input voltage u_{in}. In this process, a charge ΔQ_S flows through the input. The size of this charge depends on the state of C_S after the charge redistribution process, on the value of the input voltage and on the multiplexer. The principle with a single ADC is shown in Fig. 2.

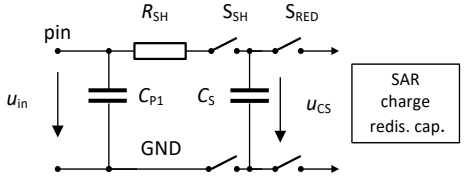

Fig. 2. Input circuit with ADC CMOS SAR.

The ADC measures a constant voltage on a single input without multiplexing. The sampling capacitor C_S is part of the charge redistribution block in the CMOS ADC, which is connected via the SRED switches.

For simplification, it can be assumed, after the charge redistribution process, a voltage remaining on the C_S, will be residual voltage U_{RES}. Very often, this voltage is equal to ½ U_{REF}, but can have a value close to zero.

In the simplified model, according to Fig. 2, the input parasitic capacitances C_{P1} at a constant value of u_{in} have a constant charge. Only C_S must be charged or discharged to the value of u_{in} again from another sample of U_{RES}. Then, with each sample acquired, charge ΔQ_s of a size according to (2) will pass through the input.

$$\Delta Q_S = (u_{\text{in}} - U_{\text{RES}})C_s \qquad (2)$$

If a constant input voltage u_{in} were measured with the sampling frequency f_{SAMP}, then according to (3), it would represent a current with an average value of I_S.

$$I_S = \Delta Q_S \cdot f_{SAMP} = (u_{\text{in}} - U_{\text{RES}})C_s \cdot f_{SAMP} \qquad (3)$$

From (2) follows, the greater the difference between input voltage and residual voltage is, the greater the charge will flow through the input at each sampling. At $u_{in} = U_{RES}$, is $\Delta Q_s = 0$, and no charge would pass through the input. This can be used for a simple experiment to determine the value of the U_{RES}, according to Fig. 3.

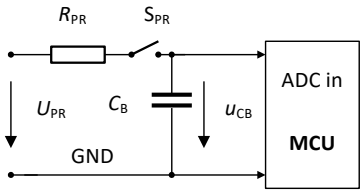

Fig. 3. Connection to determine the value of U_{RES}.

C_B with a capacity in the order of units to hundreds of nF serves as a source of a measured voltage. The smaller the capacity of the C_B is used, the more is necessary to ensure its connection to the analog input with a very short wire in order to reduce interference from the 50 Hz resp. 60 Hz. In the case of C_B = 1 nF, even the wire with a length of 10 cm will introduce a non-negligible superimposed interfering AC signal, which increases the uncertainty of the U_{RES} determination. With the S_{PR} switch opened, the MCU starts conversions of the tested ADC. After several hundred measurements, the u_{CB} voltage settles at U_{RES} value. The settling time increases with the C_B/C_S ratio. The U_{RES} value is determined by the microcontroller itself based on the data from the internal ADC.

In the MCU, the input of the CMOS SAR ADC is connected to the input pins via a multiplexer. Information about the specific solution of such a multiplexer in the MCU and its other properties and operation are usually missing from the manufacturer datasheet. Only information on the value of the C_S capacity can be found, e.g., C_{ADC} [8]. C_{ADC} expresses only the capacity of the sampling capacitor value. However, due to the multiplexor with dynamic control, according to our experiments, a non-negligible value of the capacity of other capacitors, which, due to various capacitance crosstalk from the control, must be added to this capacity as well as and also must be charged or discharged again with each sample acquired. All these capacities and the sampling capacitor C_S will be included in the simplified MCU analog input behavior model in the equivalent sampling capacity C_{SEQ}.

Based on experiments with a series of MCUs containing SAR ADCs, it was found that the behavior of ADC inputs varies by MCU design series. In some cases, with a single ADC with a simple multiplexer, the additional effect of the multiplexer is relatively small. The size of the capacity of C_{SEQ} compared to C_S can be larger in the order of units up to tens of percent. In the case of an MCU with a complex multiplexer, with, for example, a cascading principle, the difference in the size of the capacities of C_{SEQ} compared to C_S is noticeably larger. In addition, there can be even different behavior of different analog inputs connected to a different MCU input pins with a single ADC.

As already mentioned, in a multiplexer, the various capacities and crosstalk effects must be considered. For their quantification and the design of the overall analog inputs MCU model behavior in terms of input currents, experiment many sets of measurements of the charge ΔQ_S value, depending on the input voltage u_{in} value, have been performed. A measuring system with a charge amplifier was used. This allows determining the total charge passed through the selected MCU analog input at a defined input voltage u_{in} and a selected number of samples (e.g., 10 000 samples).

The results of the experiment [9] showed that for some MCUs, the input behavior can be modeled according to (2) with a small deviation.

According to the measurements of ΔQ_s, the C_S capacitance has been changed to the equivalent sampling capacity C_{SEQ}, which affects the effect of various crosstalk in the multiplex system.

$$\Delta Q_S = (u_{\text{in}} - U_{\text{RES}})C_{SEQ} \qquad (4)$$

For some MCUs, the value of C_{SEQ} was practically constant in the range of measured input voltages. For other MCUs, the size of C_{SEQ} varies with the value of u_{in} in the order of tens, sometimes even hundreds of percent, and thus showed a strong nonlinearity [7]. This concerns the ADC structure in a particular MCU, which is entirely unknown to the standard user. Therefore, measurement of the internal ADCs properties to create a simple model of the behavior of the analog inputs has been done. For example, a model described according to (4) showing the equivalent sampling capacity C_{SEQ} and its dependence on the input voltage. The aim is to roughly estimate ADC input behavior limits when working with signal sources with non-negligible internal resistance. With a constant

input voltage sampling, an RC transient occurs. The time constant is determined by the total resistance between the source u_{in} and the sample and hold circuit, expressed by the equivalent capacity of C_{SEQ}. Suppose the maximum value of C_{SEQ} is used in the calculation for a given internal resistance of the measured signal source. In that case, the correct function is ensured over the entire range of input voltages. If only the C_S given by the datasheet is used in the design, which is usually smaller than the C_{SEQ} due to not including the multiplexer properties, non-negligible measurement errors could occur in some cases. It can lead to insufficient sampling time due to the settling time of the transient during sampling or problems with the load of the measured circuit with a greater current, according to (3).

The previous text considered only a single input ADC voltage measurement. However, multiplexing and multi-channel measurement are very often used. Based on the experiments, the logical assumption that the size of ΔQ_s, or U_{RES}, due to parasitic capacitances in the multiplexer also changes with the magnitude of the voltage on the channel, which was measured in the previous multiplexer cycle. In general, a greater previously measured voltage increases the value of the U_{RES} voltage for measurements in the current channel. It also applies in the opposite direction, with a smaller voltage reducing the value of the U_{RES}.

A standard MCU user interested in the behavior of their analog inputs is not expected to be concerned with such detailed measurements with specialized charge amplifier measurement equipment. Therefore, simplified methods that are available without the need for specialized equipment, only by using the appropriate code in the MCU, have been taken into account. The validation of these simple methods of determining the C_{SEQ} was with using measurements by specialized equipment with a charge amplifier. It has been shown that even simple methods can provide information for assessing the behavior of ADC inputs in terms of input currents during the measurement. An experiment will again use the arrangement according to Fig. 3.

To verify the fact, the ADC input behaves according to the model in Fig. 2 and (4), an experiment with the discharge of an external capacitance can be used. By the S_{PR} temporarily switched on, the C_B capacitor is charged to the U_{PR} voltage. The U_{PR} voltage is chosen to the upper range of the ADC value. Subsequently, ADC conversions take place. Due to the action of the input, the charge according to (4) is sampled at each measurement. The situation from the experiment with the ADC input on pin #4 in the STM32G031F6P6 MCU, where C_B = 2200 pF, U_{PR} = 3.2 V is shown in Fig.4.

The voltage u_{CBn} after taking n samples by the ADC input with behavior corresponding to (4) will be defined by (5).

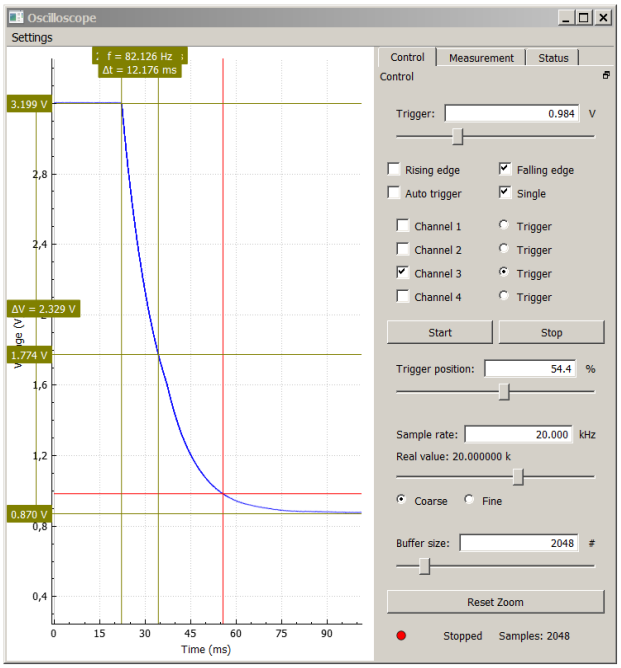

Fig. 4. Voltage at the ADC input when discharging external capacitor.

$$u_{CBn} = U_{PR} + (U_{RES} - U_{PR})\left(1 - \left(\frac{1}{1+\frac{1}{k_C}}\right)^n\right) \quad (5)$$

If the coefficient $k_C >> 1$, where $k_C = C_B/C_{SEQ}$, then the shape of the voltage u_{CBn} on C_B will approach an exponential shape, at a constant value of C_{SEQ}, at the discrete instants given by the sampling times.

The well-known relation (6) applies, similar to the value of $1/e$, where e is Euler's number, for the exponential in the time τ, here for $k_C >> 1$, corresponds to where $n = k_C$.

$$\lim_{n\to\infty}\left(\frac{1}{1+\frac{1}{n}}\right)^n = \frac{1}{e} \quad (6)$$

Thus, the number of n_{KC} samples until the voltage reaches $U_{PR} + \Delta U_{ST}/e$ to the steady value, U_{RES} determines the ratio $C_B/C_{SEQ} = n_{KC}$.

$$\Delta U_{ST} = U_{RES} - U_{PR} \quad (7)$$

In the case of a constant value of C_{SEQ}, it is sufficient to record the discretized equivalent of the transient and determine n_{KC} from it. Then to calculate C_{SEQ} from the values of C_B and k_C.

If the value of C_{SEQ} changes with the voltage, this will also affect the distortion of the exponential waveform, similar to what is seen in the record in Fig. 4.

C_B = 2200 pF was used in the experiment, the residual voltage U_{RES} = 0.87 V, and the value n_{KC} = 243. This corresponded to the capacity C_{SEQ} = 9 pF. In the datasheet, the capacity is $C_S = C_{ADC}$ = 5 pF, giving a difference of 80%. From the part below the voltage level of 1.77 V, it is clear that the size of C_{SEQ} increases even above the value

of 9 pF, which is reflected in an accelerated decrease.

A similar experiment can be performed for U_{PR} = 0 V, charging the C_B with the ADC input current. Here, C_{SEQ} reached a value of up to 12 pF. When measuring other inputs, even larger values were found.

In the experiment, according to Fig. 4, a relatively small value of capacity C_B = 2200 pF is used, which enabled the oscilloscope to record the entire waveform. Another experiment used a rather large value of capacity C_B = 100 nF, where the voltage drop was considerably slower. However, this makes it possible to determine the size of the ΔQ_s at a given input voltage. From that to, determine the value of C_{SEQ} at this selected voltage and thus replace the measurement circuits with a charge amplifier.

The experiment shows the simplified methods how to measure the size of the ΔQ_s. The correct and precise measurement method includes a charge amplifier.

To measure the total charge passed through the ADC input at N_M measurements, a setup with a charge amplifier was used. The simplified circuit diagram is in Fig. 5.

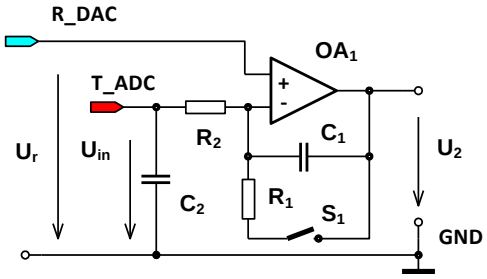

Fig. 5. Simplified circuit diagram with charge amplifier .

The control of the experiment is done using the Nucleo STM303RE kit with MCU STM32F303RE, where the DAC is used to set the voltage U_r at the input of R_DAC and the ADC to measures the voltage U_2 at the output of the charge amplifier. The used operational amplifier OA_1, MCP6002, has a negligible input current of less than 1 pA, which does not affect short-term measurements. The conversion constant of the charge amplifier is determined by the value of the capacitance C_1 = 220 nF. A quality polyester dielectric capacitor with negligible leakage current has been used. Its function is to equalize the current pulses flowing through the input of the tested ADC, to which the buffer in the output of the DAC would not be able to respond. Resistor R_2 = 4k7 has a protection function. It limits the amount of current when the voltage U_r changes and the switch S_1 is closed. The measurement process is as follows.

It the beginning, the measured ADC, whose input is connected to T_ADCA, is not sampling. A reference voltage U_r is set at the R_DAC input, at which the input charge Q_{in} will be determined. Switching the S_1 realized by the multiplexer 74HCT4053 discharges C_1. R_1 = 470 Ω limits the size of the discharge current and, at the same time, affects the time required for discharge. After opening S_1, voltage $U_2 = U_r$, neglecting the offset. The voltage U_{in} on C_2, which serves as the source of the measured voltage, then has the same value as U_r, i.e., $U_{in} = U_r$. Subsequently, the measurement of the U_{in} voltage is performed by the input of the tested ADC on the N_M samples. From the nature of the charge amplifier, the equality of the voltages $U_{in} = U_r$ results (neglecting the offset of the OA_1 and the very small voltage drop on R_2). That is, the entire measurement takes place at the defined input voltage. Due to the action of the charge passing through the input of the ADC under the test, the voltage U_2 changes

$$\Delta Q_{in} = -C_1 \cdot \Delta U_2 \qquad (8)$$

, where $\Delta U_2 = U_{2STOP} - U_{2START}$, ΔQ_{in} is the size of the total charge passed through the input of the tested ADC in the measurement process, U_{2START} is the voltage at the beginning of the measurement, and U_{2STOP} is the voltage at the end of the measurement.

The size of the charge ΔQ_s equal to one sample is determined according to (9).

$$\Delta Q_S = \frac{\Delta Q_{in}}{N_M} \qquad (9)$$

This also corresponds to the results in Fig. 6 measured using circuits with a charge amplifier, where the value of the ΔQ_s is shown as a function of the input voltage [9].

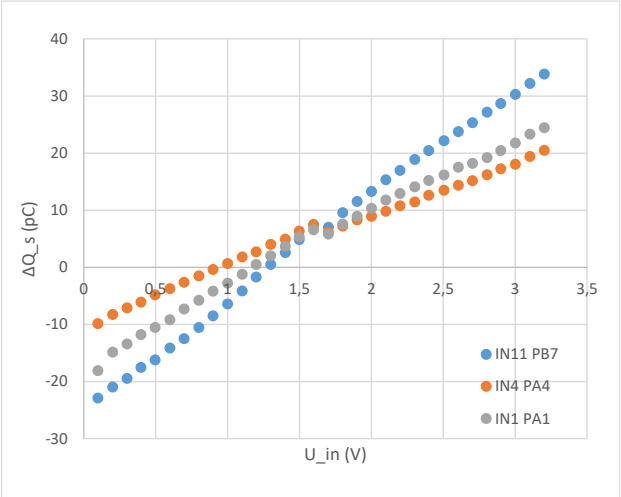

Fig. 6. STM32G031K8 ADC converter input characteristics comparison.

In the CMOS SAR ADC manufacturers' datasheets, only the value of the capacitance C_S is given, but it does not describe the complex behavior of the ADC input during the sampling. The value of the residual voltage U_{RES} is not given, and the behavior of the input during a periodic sampling, which can be roughly described by (3), is not even mentioned. Only the maximum "input leakage current" or "analog input current" value is stated. This could be, according to our experiments with a number of internal ADCs in the MCU, the size of the U_{RES} can also vary for the ADC according to the selected input of the MCU multiplexer, which can also be caused by the

cascaded multiplex system. For some MCUs, the size of ΔQ_s can change even with a deviation from the linearity given by the model according to formula (2). Thus, the sampling circuit's size of the equivalent capacitance C_{SEQ} does not have to be constant but changes with the input voltage. E.g., in the case of ADCs in STM32 series MCUs, the change in C_{SEQ} with the input voltage was from units of a percent to the increase of up to 100% in the STM32F446. However, this is still not a problem since the actual size of the input current at low sampling rates is significantly less than the manufacturer's nominal input current values.

This could be a problem when charging the sampling capacitor from a voltage source with a larger internal resistance. The smaller the sampling time is used, the smaller the internal resistance of the signal source must be. The manufacturers state this, including tables with the specific values. The problem can be when measuring the quasi-static voltage (with very slow change) on the circuit corresponding to the resistance divider according to Fig. 7, where the internal resistance of the source's measured voltage R_{TH} is greater than the value ensuring reliable charging of the sampling capacitor during the sampling.

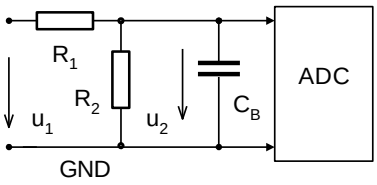

Fig. 7. Quas-static voltage measurement on the resistance divider.

Some of the online IDEs, e.g. "mbed" or "Keil studio" use a fixed setting of the sampling time, which the user cannot change for the measurement. In such a case, the solution with an auxiliary blocking capacitor C_B with a value of $C_B > 2 \cdot 2^N \cdot C_{SEQ}$, where N is the number of ADC bits, is used. In this case, C_B ensures reliable charging of the sampling capacitor. However, with periodic sampling, the size of the voltage drop on the R_{SH} due to the current I_S, see (3), must be taken into account when choosing the sampling frequency. The typical mean value of the I_S when sampling at $f_s = 100$ Hz can be in the order of nA. However, at 100 kHz, it will be in the order of µA. This value is already in the range of input currents according to the manufacturer's datasheets. Therefore, with regard to (3), it is advisable not to use the maximum sampling frequency when working with high-impedance voltage sources with the blocking capacitor C_B, as shown in Fig. 7.

III. CONCLUSION

The article presents the problems of internal CMOS SAR microcontrollers ADCs input currents, its nature and the possibility of its measurement. Based on measurements and experiments, a simplified model of the MCU analog inputs behavior was designed and verified.

This will help in the design of a data acquisition system with the MCU when measuring on signal sources with non-negligible internal resistance. Based on the mentioned procedures, it is possible to obtain data and information about the behavior of the MCU ADC, which the manufacturers do not provide in the datasheet. Mainly the value of the residual voltage, equivalent sampling capacity C_{SEQ} and its dependence on the input voltage are the parameters, which can be very important for users.

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