

Architecture of successive approximation time-to-digital converter with single set of delay lines

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Abstract – The paper addresses a time-to-digital conversion method based on successive approximation algorithm in time domain (SA-TDC). The SA-TDC is based on successive delaying the events defining a start and a stop of the input time interval being converted to a digital number by the use of binary-scaled delay components. The paper contribution is a presentation of several enhancements of SA-TDC architecture with single set of delay lines such as a reduction of hardware complexity and a decrease of quantization step by asymmetric inverter design in delay lines. On the other hand, the problem of metastability in logic appeared during conversion process for quasi-simultaneous inputs as a significant drawback of SA-TDCs is explored.

I. INTRODUCTION

The successive approximation scheme belongs to fundamental and most successful methods of analog-to-digital conversion. The first successive approximation analog-to-digital converter (SA-ADCs) was invented for commercial applications in the middle of 50s although the binary search algorithm which is a principle of SA-ADCs has been known at least since the 16th century [1]. The classical SA-ADC architecture commercially implemented today is based on successive charge redistribution in the binary-scaled capacitor array [2] and was introduced in the middle of the 70s [3].

A. General Successive Approximation Schemes

Two generic successive approximation algorithms are adopted in general to analog-to-digital conversion. The first algorithm is based on evaluating output bits on the basis of creating a discrete equivalent Y of the input value X_{in} with the use of binary-weighted increments (Fig. 1a). In each step, the discrete equivalent is compared to the input value. If a comparison shows that the equivalent is higher than the input value, then the tested bit is set to zero. Otherwise, it is evaluated to one. This method, which is commonly used for commercially implemented SA-ADCs, can be termed as the *oscillating successive*

approximation since the discrete equivalent approaches the input value alternately upward and downward (Fig. 1a).

In the alternative method, the output bits are evaluated on the basis of successive balancing of the input value by the binary-weighted increments added in each step to the reference or to the input value depending on which value is actually smaller. In the first step, the input value X_{in} is compared to the reference (R) equal to the increment corresponding to the most significant bit (Fig. 1b). In next steps, the binary-scaled increments are added to the input value X_{in} , which results in creating the balance (S), or to the reference value (R), depending on which value (S or R) is lower. In the last step, both values (S and R) differ no more than by the *LSB*. The relevant method of successive approximation is referred in the present study as the *monotone successive approximation*. The monotone algorithm is even simpler than the oscillating successive approximation because possible reversals of addition operations needed to create discrete equivalents of input value are avoided. There are implementations of the monotone successive approximation scheme for analog-to-digital conversion in the voltage domain [4].

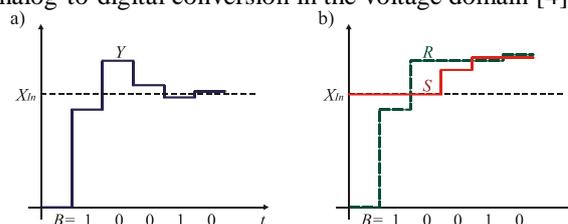


Fig. 1. Oscillating (a) and monotone (b) successive approximation algorithms.

B. Successive Approximation in Time Domain (SA-TDC)

The distinctive feature of the monotone successive approximation is that no binary-scaled increment is removed after comparison. This feature makes possible the use of the successive approximation principle to convert signals represented by physical magnitudes that are inherently monotone increasing (e.g. time). The oscillating approximation scheme is applicable for

indirect time-to-digital conversion with prior translation of the time interval to the other domain (e.g., charge) that handles subtraction operation [5], [6], [16]. The adoption of the monotone approximation scheme to signals encoded in time resulted in a development of successive approximation time-to-digital converters (SA-TDCs) where the conversion is realized strictly in the time domain [7]-[13].

According to the monotone successive approximation, the principle of SA-TDC is based on successive delaying the events defining a start and a stop of the input time interval being converted by the use of binary-scaled delay components. In each step, the corresponding delay is always added to the earliest event arriving, so that the outputs from the last cell will be closer in time than the minimum delay increment *LSB*.

The concept of the SA-TDC has been introduced in patent description [7]. The technique of SA-TDCs was further developed in [8]-[13]. In the SA-TDCs the binary-scaled time increments are produced by delay lines [8], [9] or delay difference between logic states [10]. The experimental results of the SA-TDC based on a difference between latencies introduced by lines with a fixed and programmable delay are reported in [10]. The resolution of relevant converter implemented in 0.35 μs CMOS technology is 1.22 ps with the range of 327 μs . The recent work presents the SA-TDC with sub-ps-level resolution [11]. As opposed to simple clock-based TDCs (e.g., [15]), the SA-TDC algorithm is characterized by a *redundant conversion time* which in addition depends on the input time interval being converted. This feature makes the SA-TDC similar to self-timed analog-to-digital converters based on event-driven successive charge redistribution [5], [6], [16].

Various variants of SA-TDC architecture including feedback-based models with propositions of optimized configurations have been studied in [17]. One of optimizations discussed in [17] is removing redundancy of programmable delay lines that allow to reduce the complexity of hardware blocks used in SA-TDC design. The present paper continues discussion on the SA-TDC architecture with single set of delay lines introduced in [17]. The paper contribution is a presentation of several enhancements such as further reduction of hardware complexity and improvement of quantization step by asymmetric inverter design in delay lines. On the other hand, the problem of metastability in logic appeared during conversion process as a significant drawback of SA-TDCs has been explored.

II. BASIC SA-TDC ARCHITECTURE MODEL

The basic architecture of the n -bit SA-TDC architecture for a digital evaluation of a position in time of the signal event (S) in relation to the reference event (R) is shown in Fig. 2.

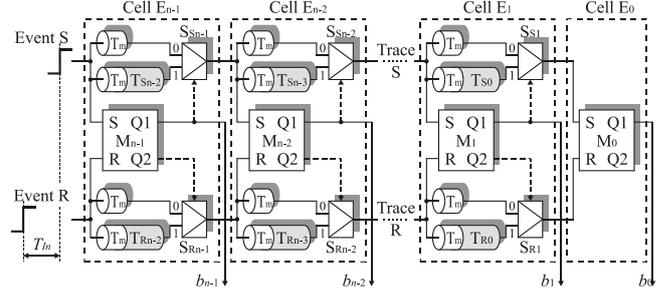


Fig. 2. Architecture of SA-TDC architecture.

The presented architecture in Fig. 2 is adapted to produce both positive and negative (*i.e.*, bipolar) digital codes depending on the chronology of the events. The example of the *event* is an edge of a pulse signal.

The SA-TDC contains two traces, R and S , respectively for propagation of the reference event (R) and of the signal event (S). The converter is built of a sequence of cells E_{n-1}, \dots, E_0 and each cell corresponds to an output bit in the order from MSB to LSB. The cells E_{n-1}, \dots, E_1 are symmetrical and each of them comprises the MUTEX block M_i providing a mutual exclusion operation, a pair of delay lines (T_{Ri}, T_{Si}) and a pair of multiplexers (S_{Ri}, S_{Si}) controlled by the output of the MUTEX M_i , where $i=1, \dots, n-1$. The cell E_0 comprises just the MUTEX M_0 . The propagation delay of the MUTEX M_i , the time of multiplexers switching (S_{Ri}, S_{Si}) and of stabilization of a state on their outputs are compensated by elements providing extra delay T_m .

Both events S and R are propagated by the sequence of cells from E_{n-1} to E_0 . The role of each cell is twofold. First, each cell has to identify which event, S or R , arrives to the input of the cell sooner. Second, the cells E_{n-1}, \dots, E_1 are aimed to delay an earlier event by the delay component corresponding to the position of the cell. Delays provided by delay lines in cells with higher indexes are doubled with each cell and the *LSB* delay (T_0) is introduced by the cell E_1 . In particular, the delay T_{n-2} provided by the cell E_{n-1} corresponds to one-quarter of the full scale. The cell E_0 does not contain any delay line since the aim of the final SA-TDC conversion step is just to detect chronology of events arriving to inputs of this cell.

The detection of an earlier event is realized by the MUTEX block that comprises of a RS latch and a filter that prevents the MUTEX outputs (Q_1 and Q_2) from metastable states that may remain on the RS latch outputs (O_1 and O_2) (Fig. 3). In the idle state when the level of the signals in both traces S and R is low, the outputs Q_1 and Q_2 of the MUTEX M_i is kept low. If the reference edge R arrives to the cell E_i first, the output Q_2 of the MUTEX M_i is set to one because the trace R feeds the *Reset* input. If the signal edge S precedes the reference R , the output Q_1 is set to one. The output signal of the MUTEX M_i causes switching one of multiplexers, S_{Ri} or S_{Si} , that corresponds to the event arriving to the cell E_i first, in

order to direct the leading signal to corresponding delay line ($T_{S_{i-1}}$ or $T_{R_{i-1}}$). Each cell uses only one delay line in a given conversion process.

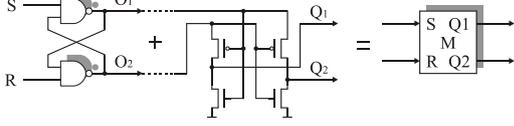


Fig. 3. Diagram of MUTEX block.

III. SA-TDC WITH SINGLE SET OF DELAY LINES

The classical architecture of the SA-TDC may be optimized in terms of a reduction of functional blocks [17]. The observation behind simplifying the classical architecture is that each cell introduces a corresponding delay only to one track (S or R). Therefore, the use of two delay lines in each cell is redundant. The corresponding circuit configurations with cells containing only a single delay line is presented in Fig. 4 [17]. One delay line in each cell E_i might be simply eliminated by the introducing two extra two-to-one multiplexers.

In Fig. 4, the delay lines are located in the trace R . The role of the input multiplexers S_{Si} , S_{Ri} , $i=0, \dots, n-1$ is to direct the earlier signal edge (S or R) to the delay line T_{i-1} included in the cell E_{i-1} . On the other hand, the output multiplexers S_{SOi} , S_{ROi} are aimed to guide the signal appeared on the output of delay line T_{i-1} to the relevant trace (signal S to trace S and reference R to trace R) (Fig. 5).

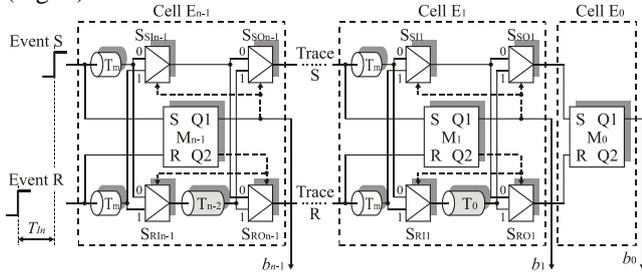


Fig. 4. Architecture of SA-TDC with single delay line.

Elimination of one delay line from each cell (Fig. 4) compared to basic architecture (Fig. 2) is achieved at the price of introducing an extra pair of multiplexers. The substitution of delay line by two multiplexers is profitable especially for the cell corresponding to the MSB. For example, in the 8-bit converter, the MSB delay line (T_6) is built of 256 transistors whereas a pair of multiplexers contains just 28 transistors. Thus, the SA-TDC architecture with a single set of delay lines is undoubtedly more efficient in terms of chip die area. However, an introduction of extra multiplexers to the traces S and R creates a source of additional conversion errors because the propagation delay of the multiplexer in the stable state differs from the propagation delay of the multiplexer whose output has been switched just before. Therefore, a development of enhanced converter architecture with single set of delay lines and one pair of multiplexers in

each cell is highly desired.

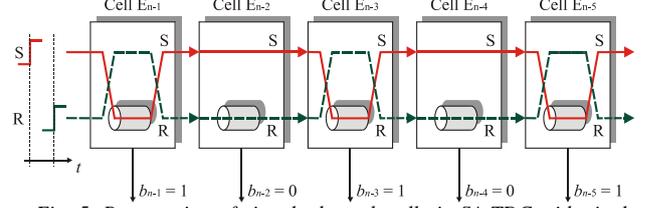


Fig. 5. Propagation of signals through cells in SA-TDC with single set of delay lines according to principle that signals S and R arrive to cell inputs consequently in relevant traces S and R .

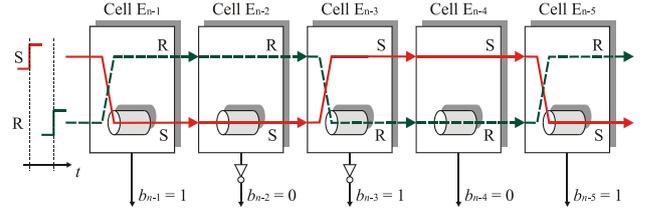


Fig. 6. Propagation of signals in SA-TDC with single set of delay lines without output multiplexers with appropriate inversion of output bits.

As we will show now, a simple observation of SA-TDC conversion algorithm allows to remove output multiplexers S_{SOi} , S_{ROi} from each cell while still using a single set of delay lines. It is because the correct evaluation of SA-TDC output bits is still possible even if the signals S and R are not propagated consequently through relevant traces S and R . Note that if the output multiplexers S_{SOi} , S_{ROi} are removed, the MUTEX block in the next cell E_{i-1} still guides the leading edge to the delay line correctly. But the output of this cell provides an inverted state of a particular output bit in case if the signals arrive to the cell in opposite traces.

The corresponding principle is illustrated in Fig. 6. Assume the edge S precedes the edge R at the input of the cell E_{n-1} . Then, the MUTEX M_{n-1} (see Fig. 3) sets the MSB (b_{n-1}) to one and the signal S is guided to the delay line T_{n-2} which is located in the trace R . If the output multiplexers $S_{SO_{n-1}}$, $S_{RO_{n-1}}$ are absent, then the signal S appears in the trace R at the input of the cell E_{n-2} . Assume the edge S (transmitted in trace R) follows the edge R (in trace S) at the input of E_{n-2} . Then, the output state Q_{n-2} of the MUTEX M_{n-2} is set to one. However, the bit b_{n-2} should be evaluated to zero because the signals S and R are at the inputs of E_{n-2} altered (Fig. 6). Therefore, the output state Q_{n-2} of the MUTEX M_{n-2} has to be inverted to represent the output bit b_{n-2} . The inversion of MUTEX output Q_{n-3} in the cell E_{n-3} is also required to get the bit b_{n-3} because the signals S and R at the inputs of E_{n-3} appear also in opposite traces (Fig. 6). The inversion is not needed to produce the output bits b_{n-4} and b_{n-5} because the positions of signals S and R at inputs of E_{n-4} and E_{n-5} are correct.

Generalizing, a state of a given output bit has to be inverted if the signals S and R arrive to the cell inputs in opposite traces. The correction relates never to the MSB (b_{n-1}) because the signals are provided to SA-TDC inputs

by the assumption correctly. Furthermore, the signals S and R are altered in traces when propagated successively through the cells if there is a need to change the signal being delayed in the delay line. Thus, the signals appear in opposite traces when the number of trace altering is odd. The conclusion is that the inversion is needed for these output bits that are between odd and even occurrences of the state ‘one’. A task of detection of odd occurrences of output bits equal to one can be carried out by a simple encoder whose diagram is shown in Fig. 7. Each cell except E_{n-1} must be equipped with XOR gates. Depending on the implementation scheme, each XOR gate requires from 6 to 16 transistors that substitute 28 transistors needed to build a pair of output multiplexers S_{SOi} i S_{ROi} (Fig. 4). In E_{n-1} , XOR gate is not required (Fig. 7).

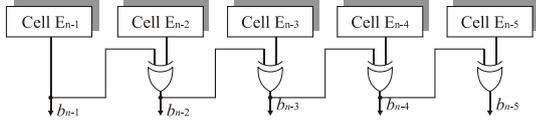


Fig. 7. Encoder for correction of output bits.

The proposition of a final architecture of the SA-TDC with single set of delay lines is presented in Fig. 8. The advantage of this architecture is not only a reduction of transistors used for implementation of logic elements but also a placement of these elements outside traces S and R . The latter is a significant benefit for converter accuracy because it allows to eliminate an influence of logic propagation delays on latency introduced by delay lines.

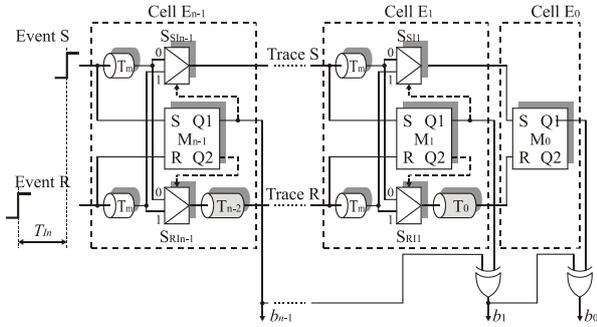


Fig. 8. Optimized architecture of SA-TDC with single set of delay lines.

IV. ASYMMETRIC INVERTER DESIGN

The delay lines in the SA-TDCs are built of a cascade of inverter pairs [8]-[13]. Basically, the propagation delay of a single pair of inverters defines a quantization step T_0 of SA-TDC architectures. The propagation delay of classical (symmetric) inverter designed using standard CMOS 180nm technology (UMC180) is 49,6 ps which gives quantization step equal to $T_0 = 99,2$ ps [9], [18].

We propose to reduce the quantization step of the SA-TDC by optimizing the inverters to transfer quickly active signal edges. The motivation behind optimizing inverter design is that SA-TDCs are usually adopted to convert input time intervals defined by the signal edges of

a specific type (*i.e.*, rising or falling). The type of the active edge is determined by MUTEX design (Fig. 3). In particular, if RS latches in MUTEX blocks are built of NAND gates as assumed in the present study, the active edge is rising. In case of using NOR gates in MUTEX, the active edge is falling.

We have designed the inverters in delay lines by asymmetric shaping transistor dimensions (W/L ratio). The first inverter is adopted to transfer quickly a rising edge whereas the second inverter is aimed to introduce a minimum delay for a falling edge (Fig. 9). The asymmetric design consists in introducing sufficient disparity of the W/L ratio between transistors in the pair as shown in Table 1. To accelerate propagation time of the first inverter in a pair for rising edges, the W/L ratio of transistor P1 being switched off is around one whereas it is of the order of tens for transistor N1 being switched on. The W/L for transistors in the second inverter (N2, P2) are scaled conversely since they are optimized to propagate quickly falling signal edges.

The simulative investigations show that the quantization step T_0 can be reduced to about 24.4 ps for the technology UMC180 by introducing asymmetry of an inverter pair. In Table 1, the transistor dimensions that allow to achieve T_0 around 25 ps (24.98 ps) are listed. The reduction of the propagation delay for the active edges (Fig. 10a) is obtained at the price of extending the delay for inactive edges (Fig. 10b). However, the latter is not disadvantageous except certain increase of minimum space required between consecutive conversion cycles.

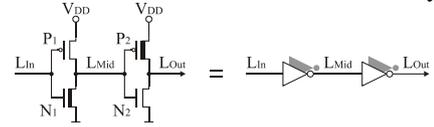


Fig. 9. Asymmetric design of inverter pair in delay lines.

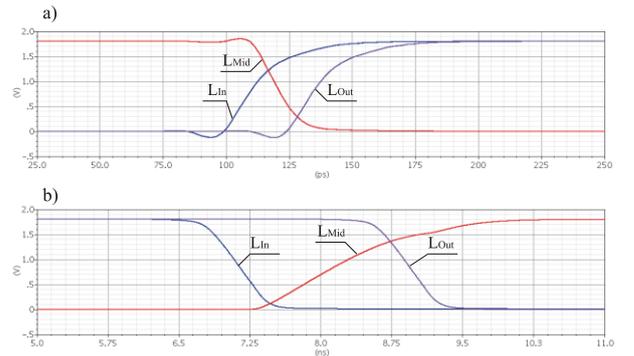


Fig. 10. Voltage signals at input (L_{in}), in the middle (L_{mid}) and on output (L_{out}) of inverter pair (see Fig. 9) in delay line for active and inactive signal edges.

Tab. 1. Parameters of transistors in asymmetric inverter pair (Fig. 9).

	P ₁	N ₁	P ₂	N ₂
W [μm]	0.27	12.22	18.00	0.27
L [μm]	0.18	0.18	0.18	0.18
Fingers	1	47	1	1

V. METASTABILITY ON MUTEX OUTPUT

As discussed extensively before, the conversion of SA-TDC consists in successive delaying the signals S and R by the use of binary-scaled latency components introduced by delay lines. However, the signals S and R that are propagated not only via delay lines but also through logic elements, that is, the multiplexers S_{Si} and S_{Ri} and extra delay components T_m (Fig. 8). The latter are aimed to compensate the logic propagation delays and in this way to resolve metastability with high enough probability (Figs. 2 and 8). The time of propagation of a signal through delay components T_m must be sufficiently long to allow the MUTEX to react to a leading edge of the signal and to switch and stabilize a new state on the multiplexer output. In [18], the delay T_m is set to 500 ps.

The major component of the T_m is a propagation delay (response time) of the MUTEX block which grows if the active edges of the signals S and R are close in time one another when they arrive to the cell inputs. If both edges arrive almost simultaneously, the RS latch needs a long time to settle which edge arrived first. During that time, the metastable state remains on both RS latch outputs which is clearly presented in Fig. 11. The filter on the output of the MUTEX block prevents the MUTEX outputs Q_1 and Q_2 from metastable states (Fig. 3) but it is unable to reduce the MUTEX propagation delay.

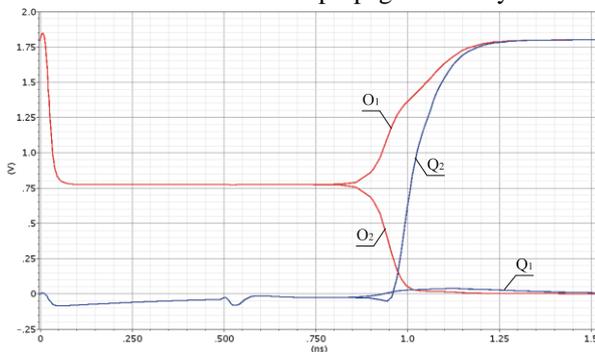


Fig. 11. Signals on RS latch outputs (O_1 and O_2) and MUTEX outputs (Q_1 and Q_2) when edges of signals S and R arrive simultaneously.

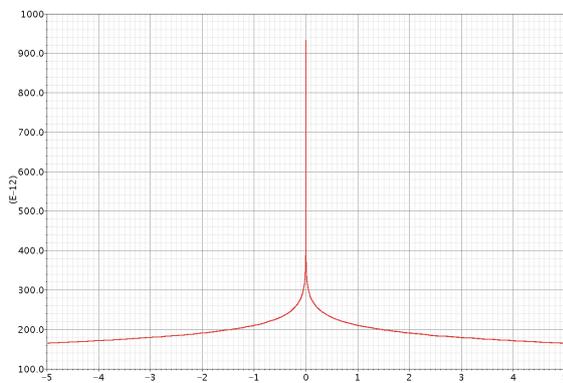


Fig. 12. Propagation delay of MUTEX versus delay between active edges of the signals S and R .

The relationship of the propagation delay of the

MUTEX versus the delay between active edges of the signals S and R is presented in Fig. 12. The plot of this relationship cannot be interpreted quantitatively but only qualitatively because an increase of precision of simulation experiment causes further extension of evaluation of the MUTEX propagation delay for quasi-simultaneous signals on its inputs. If the transistors used for MUTEX design are not ideally symmetrical, the metastable state of maximum duration occurs for non-zero delay between signals on its inputs.

Even a significant increase of T_m delay is unable to eliminate the possibility of long metastable states on RS output. It is worth to note that the active edges of the signals S and R can arrive almost simultaneously to each cell, that is, in any stage of the conversion cycle. The occurrences of such situation might cause conversion errors significantly greater than T_0 that corresponds to LSB . Thus, the metastability on output of logic elements is a serious disadvantage of the SA-TDCs.

VI. CONCLUSION

In the paper, further propositions of enhancements of the SA-TDC feedforward architecture with single set of delay lines are presented. First, the relevant enhancements allow to reduce hardware complexity and chip die area. Second, a reduction of quantization step of the SA-TDC is achieved by asymmetric inverter design in delay lines that results in quick propagation of active signal edges. Although the decrease of the propagation delay of active edges is gained at the price of an increase of the latency for inactive edges of the signal, this effect is of secondary importance in converter operation. On the other hand, the problem of metastability in logic appeared during conversion process as a significant drawback of SA-TDCs has been explored. The analysis presented in the paper has been validated by simulation results of SA-TDC implementation in CMOS (UMC) technology with the feature size of 180 nm.

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