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USB-INTERFACED DSP-INSTRUMENT FOR POWER QUALITY ANALYSES

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Abstract- In the paper, the characterization of designed and implemented high-performance real-time power quality measuring instrument is discussed. After a description of the hardware, firmware, power quality analyzer software and USB based data transfer mode, the paper continues with the discussion on a set of preliminary performances tests. In particular a set of test based on dip measurement and Total Harmonic Distortion measurement have been made and will be reported.

I. Introduction

Main problems in definition of instrument features for PQ monitoring come from the divergent requirements that different PQ analysis has. Since, such disturbs are of various nature and are caused from different phenomena, are difficult to monitor. In particular, some phenomena (such as a transients) require a very fast analysis in short time interval, while others (such as flicker) are assessed over longer time intervals (10 minutes for Pst index and an hour for Plt index). The standards that give the closest references to power quality phenomena are in the IEC 61000 family. In particular these standards establish also the data acquisition attributes necessary to characterize different power quality phenomena [1]-[3]. In order to address the monitoring standard requirements, a real time digital instrument, based on DSP architecture was (already) designed and realized. In the proposed instrument, specific algorithms for each one of PQ phenomenon are developed, referring to the standard. In the following the test procedures for the characterization of whole instrument are reported and discussed with the aim of highlighting the performance of realized device.

II. PQ Instrument

A scheme of the proposed PQ analyzer is shown in figure 1. It is mainly composed by a data processing block and a communication front end. The data processing section is formed by the DSK TMS320C6713 that stores a C6713 floating point Digital Signal Processor (DSP). This DSP works with a clock of 225 MHz, based on VLIW (Very Long Instruction Word) architecture, where the transfer mode of data and programs is made through two separated buses. Moreover the DSK has an External Memory Interface (EMIF) that allows the interface between internal memory of DSK and external devices, such as ADC. The presence of a EDMA (Enhanced Direct Memory Access) allows the direct storage of samples, by avoiding the delay caused from the access in memory of the processor.

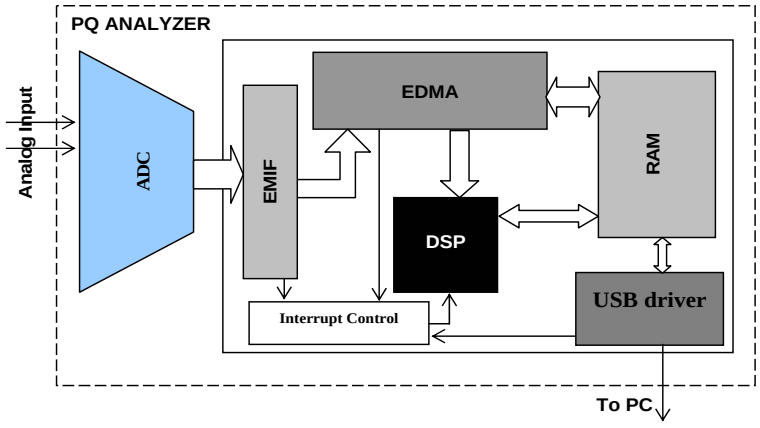

Fig.1: Real time instrument block diagram

The acquisition section is composed by an ADC THS1206 with a resolution of 12 bit and a max sampling rate of 6 MSps. This ADC has 4 multiplexed single-ended channels with synchronous sampling. An internal 16-word FIFO is used for direct interface with DSP. The communication section is composed by USB DSK-internal device to implement the communication between target DSP and a local PC to allow the instrument control and output data exchange.[4].

A. Power Quality Algorithms

The structure of the software instrument implementation is schematically shown in figure 2. The samples can be acquired with a max sampling frequency up to 1 MSps. The time domain algorithm adopted is fully described in [6]. This section is directly connected with a flagging event register.

The data managing section has the task to store and manage the data in three buffers, through an EDMA controller, to send the interrupt to DSP to process the new data, and to distribute the data in different dimensions to the frequency detection section (1 cycle), to the harmonics analysis section (10 cycles), to the RMS section (one sample), and so on.

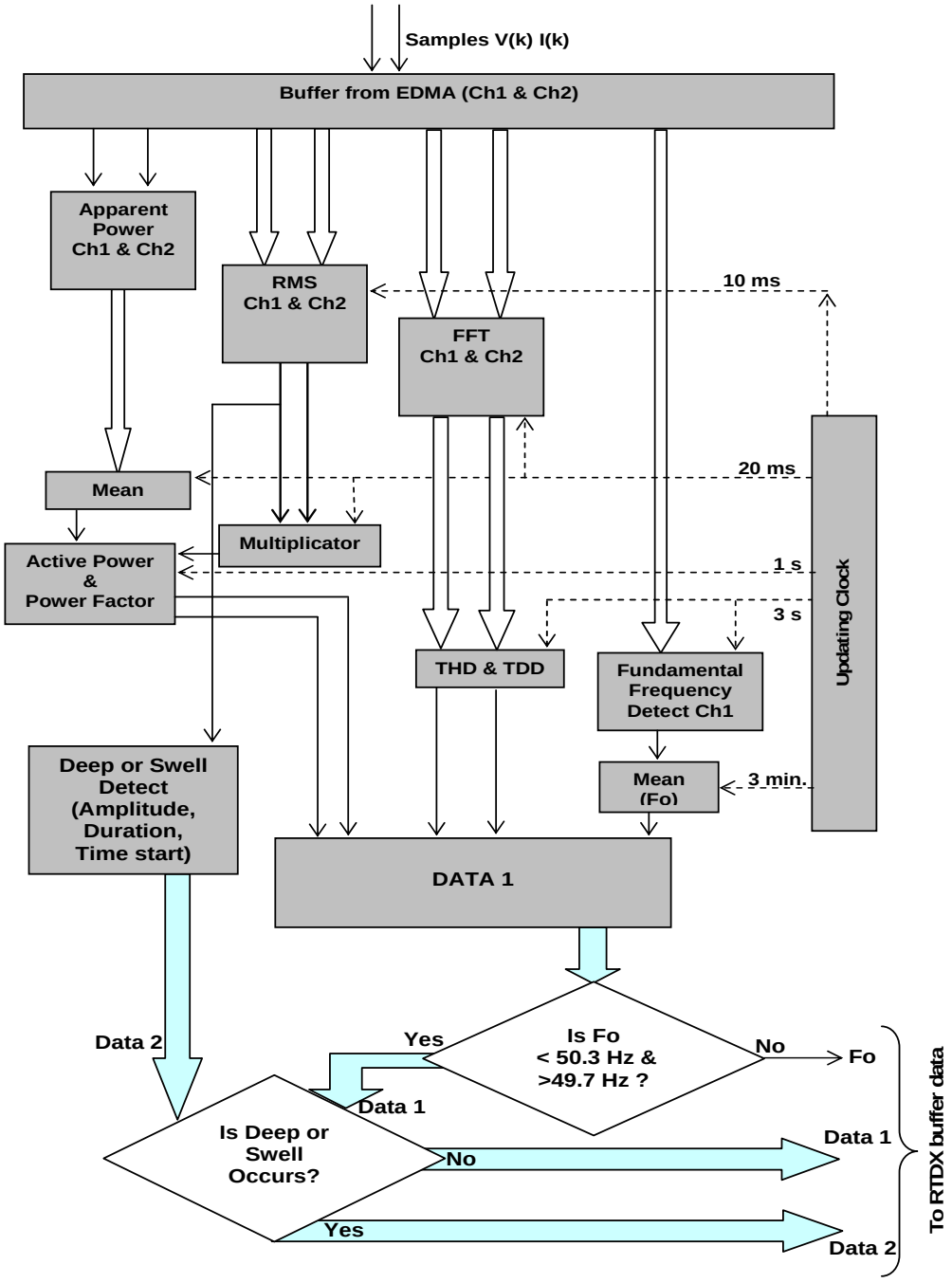

Fig. 2: PQ algorithm diagram

The fundamental frequency detection routine is one of the most important algorithms. This section is essential to implement some analyses, according to reference standards, and to estimate the fundamental frequency deviation. The synchronization of the input sequence is implemented by two main sections: i) hysteresis threshold block that selects a number of samples between the first and the second zero crossing; ii) least square linear regression block, that rebuilds the real index position of the input samples zero crossing by means of linear regression technique.

The RMS algorithm adopts a sliding window technique, where the RMS value, calculated for each new sample, is estimated through the previous RMS value, the new sample and the oldest sample stored in the buffer in one cycle of fundamental frequency and presented each half period of fundamental frequency.
The THD index (Total Harmonic Distortion) is calculated through the following equation:

$$THD(\%) = \sqrt{\frac{\sum_{i=2}^{\frac{M}{2}-1} \left[\left|FFT_M\left(x(k)\right)(i)\right|\right]^2}{\left|FFT_M\left(x(k)\right)(1)\right|}}.100 \longrightarrow M = \frac{10\,fc}{fo} \qquad (1)$$

The results of all the measuring sections are validated relying the flagging concept [2]. Not flagged data are grouped with reference to absolute time.

B. Communication algorithm

in this section will be describe two algorithms (host side and target side) implemented for the local data communication, through Real Time Data eXchange, between PC and DSK.
The RTDX (Real-Time Data Exchange) is a set of low-level instructions that allow the implementation of a base communication protocol between the DSP and the PC. The Communication between the two entities should be done in a transparent mode and without compromising the DSP analysis, but nevertheless must be continuous and in real-time way.
To transmit data from host to target it is necessary to declare an input channel on the target side. The target requires the data through the channel input using a dedicate routine. This request is recorded in a buffer target and then sent to host through the JTAG interface. All data, to be sent to target, are written in a buffer declared in the RTDX library. The data are then written into the memory location chosen by target, in Real-Time way. Then, The host notification to the target when the transaction is completed.
A particular procedure, known as RTDX Exported Interface, enable features for RTDX access by a host client. By using these functions, the application can obtain data from RTDX Host Library or send data to Host RTDX Library.
The RTDX Exported Interface is a "dll" imported at the beginning of the host program and contains an additional method that allows to select a specific board and processor.
On the target side, the first operation to do is that to reserve memory locations for RTDX program and RTDX data.

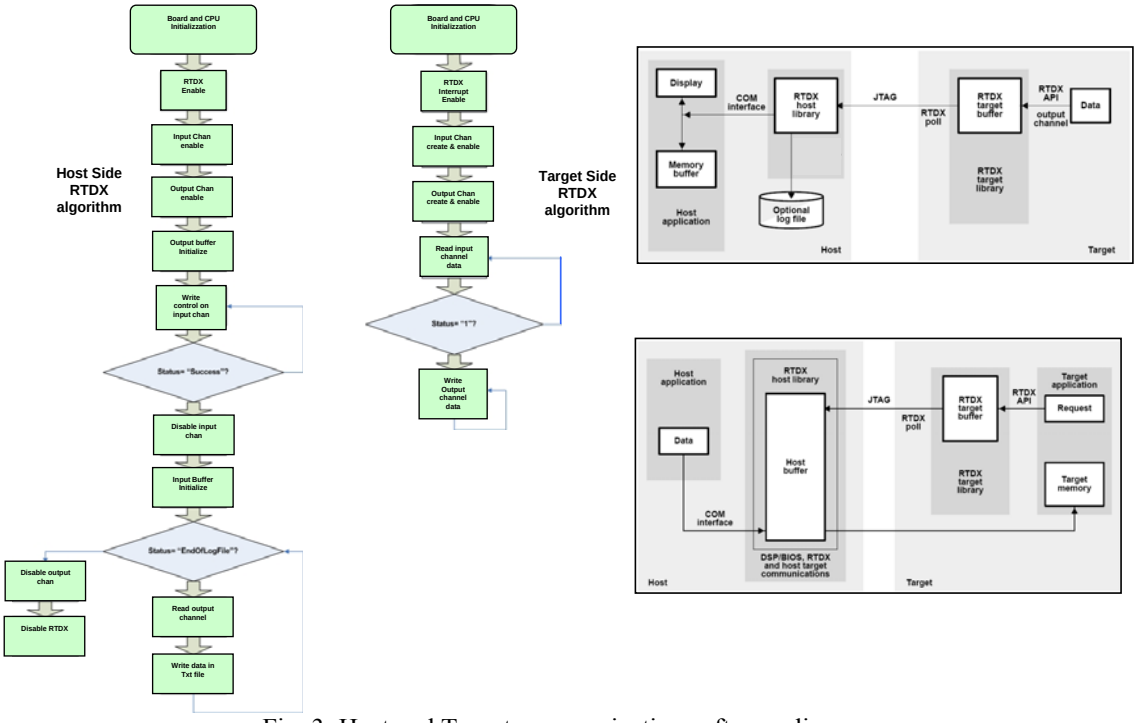

Fig. 3: Host and Target communication software diagram

The data in transfer protocol are composed by five elements, where each one is a double type and so the string is formed by 20 Byte. Each element, if no events occur, describes in order: THD, TDD, Active Power, Power Factor,

Fundamental Frequency, like it is possible to view in figure 4a. If the "dip event" occurs, the data string become as figure 4b. Where the first element indicates the event duration, the second element indicates the minimum value of the RMS voltage, the third and fourth elements are configured as 00 to indicate that the event is a dip, while the last element is not considered.
In "swell" case the first element has the same mean of the "dip" case, and so indicates the event duration. The second element describes the maximum value of RMS voltage, while the third and fourth elements are configured as 11 to indicate that the event is a "swell". Such as in the precedent case, the last element is not considered (figure 4c).

THD	TDD	Act.Pow.	Pow.Fact.	Fund. Freq.

Fig. 4a data string

Duration	Min	0	0	-

Fig. 4b data string

Duration	Max	1	1	-

Fig. 4c data string

III. Performances test

In order to characterize the implemented measuring system, some experimental tests are reported. These tests are made to highlighting the performance of a single algorithm of the whole instrument. In particular way, a set of test on dip measurement and THD measurement are followed showed.

C. Measurement station

The test station, adopted for performance verification of PQ analyzer, is composed by a signal generator, implemented in CVI environment, that drive a Pacific Power source (drove) AMX3120. The Norma D6000 is used to verify the signals generated. The measurement station is completed by the instrument under test and by a personal computer, that receives results through a Real Time Data Exchange (RTDX) channel on USB and displays them. The Measurement station is shown in figure 4.

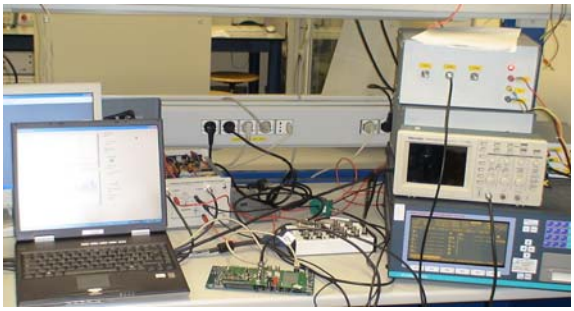

Fig. 5: Measurement station

$$\overline{THD}(\%) = \frac{1}{N}\sum_{i=0}^{N-1} THD\%(i) \longrightarrow N = number\ of\ experiments \qquad (2)$$

$$\delta THD(\%) = \sqrt{\frac{\sum_{i=0}^{N-1}\left(THD(i) - \overline{THD}\right)^2 + \sum_{i=0}^{N-1}\left(THD(i) - THDth\right)^2}{(N-1)}} \qquad (3)$$

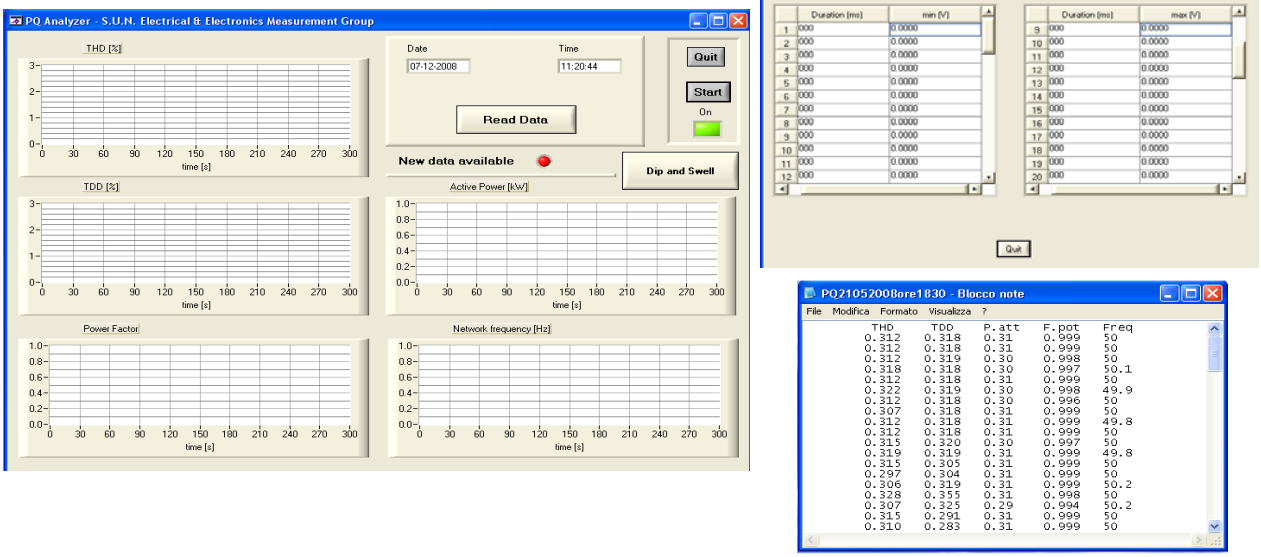

Fig. 6 Instrument User Interface

In figure 6, are showed, respectively, the user interface that runs on local PC host, where it is possible manages, stores and displays the DSP processed data, the dip and swell events table list, and a set of processed data, stored in text file and formatted like described on previous paragraph.

D. Dip test

The Voltage RMS evaluation, is made by using the sliding window technique. This technique permits to process the data each new acquired sample and then refresh the result each half period of fundamental frequency, according to IEC standard. The dips test is composed by three different tests, respectively to the 20% (test 1), to the 40% (test 2) and to the 60% (test 3) than nominal voltage (230 Vrms), and with duration of 0.11, 0.35, 5.25, and 15 second. The disturbance is generated trough the signal generator on Power Source, driven by CVI platform. The results, aggregated in the follow tables, show that the relative duration deviation is always lower than 1%, while the relative voltage minimum deviation is lower than 0.5%.

Table I dip test 1

Test	Duration	Measured Duration	εr Voltage Value	εr Duration
1.1	0.11s	0.111s	0.01%	0.9%
1.2	0.35s	0.349s	0.01%	0.1%
1.3	5.25s	5.221s	0.01%	0.4%
1.4	15s	14.976	0.01%	0.16%

Table II dip test 2

Test	Duration	Measured Duration	εr Voltage Value	εr Duration
2.1	0.11s	0.111s	0.5%	0.9%
2.2	0.35s	0.348s	0.5%	0.6%
2.3	5.25s	5.222s	0.5%	0.5%
2.4	15s	14.976	0.5%	0.16%

Table III dip test 3

Test	Duration	Measured Duration	εr Voltage Value	εr Duration
3.1	0.11	0.112	0.3%	0.18%
3.2	0.35	0.349	0.3%	0.1%
3.3	5.25	5.221	0.3%	0.4%
3.4	15	14.976	0.3%	0.16%

E. THD test

The harmonic content is measured by THD through the equation (1). The results are averaged on 1000 measurements for each signal generated, and for each test are estimated the mean deviation, between measured and theoretical THD, and the uncertainty as shown in equations 2 and 3.
The table IV shows the results of tests, made with fundamental and an harmonic, with amplitude spanning from 1% to 14% with step of 1%, until the 7th order. The table V contains the results of the tests made with a single harmonic, with amplitude of 10% respect to the fundamental amplitude, until 7th order and with the phase variable between 0° and 180°. In table VI are reported the results of test where the fundamental frequency is varied between 49.75 Hz and 50.25 Hz, with a step of 0.25 Hz, and with an 10% second harmonic.

IV. Conclusions

In the paper, a preliminary characterization of developed Real Time PQ analyzer, was made. After a description of system, in term of devices chosen, of peripheral settings, of data acquisition management and data transfer mode, and of power quality analyzer software, it was shown the characterization of synchronization algorithm. Then, some experimental results to characterize the system, in terms of time domain and spectral analyses, have been reported. In particular test on voltage dips and THD, in terms of mean error dependent on harmonics amplitude, phase and frequency fundamental deviation have been reported. The dip tests and the THD tests show like the instrument has the good performances in term of relative deviation, in fact the errors in time domain analyses and in frequency domain analyses are lower than 1% such as an class A instrument.
In the future more tests to characterize the system performances will be reported.

	Harmonic order					
	2	3	4	5	6	7
Distortion %	Absolute deviation between measured and theoretical THD					
1	-0.02620	0.06260	-0.016	0.0111	-0.0112	0.0082
2	-0.01150	0.06350	-0.0122	0.0216	-0.0153	0.0252
3	-0.01020	0.06600	-0.0132	0.0375	-0.0104	0.0127
4	-0.01380	0.08200	-0.0144	0.0398	-0.0093	0.0307
5	-0.0149	0.06690	-0.0141	0.0306	-0.0153	0.0286
6	-0.01600	0.06700	-0.0179	0.0544	-0.0257	0.0183
7	-0.0279	0.07110	-0.0273	0.0114	-0.0222	0.0091
8	-0.02080	0.06010	-0.0396	0.0386	-0.0135	0.0357
9	-0.0277	0.05950	-0.0345	0.0197	-0.0275	0.0037
10	-0.03170	0.03240	-0.0354	0.022	-0.0333	0.018
11	-0.0258	0.07510	-0.0389	0.0229	-0.0273	-0.0131
12	-0.0392	0.03100	-0.0403	0.0343	-0.0338	0.0095
13	-0.04	0.06260	-0.0385	0.0094	-0.0272	-0.0165
14	-0.0312	0.05680	-0.0333	0.019	-0.0348	0.004

TABLE IV-THD measurement results-amplitude test

	Harmonic order					
	2	3	4	5	6	7
Phase(°)	Absolute deviation between measured and theoretical THD					
0	-0.0317	0.0325	-0.0354	0.022	-0.0333	0.018
15	-0.0296	0.0437	-0.0233	0.0183	-0.0238	-0.0022
25	-0.0218	0.0457	-0.0222	0.0082	-0.0221	0.0154
45	-0.0164	0.0405	-0.0176	0.0148	-0.0108	0.0083
75	-0.0023	0.0158	-0.0064	-0.0008	-0.0058	-0.0122
90	-0.0059	-0.0052	-0.0042	-0.0041	0.0014	-0.0044
120	-0.0003	-0.0492	-0.011	-0.0278	-0.0134	-0.0196
150	-0.0251	-0.0919	-0.0185	-0.0548	-0.0157	-0.0483
180	-0.0317	-0.0982	-0.0354	-0.0854	-0.0333	-0.0537

TABLE V-THD measurement results-phase test

Fundamental frequency (Hz)	Error(%) unsyncro.	Error(%) syncro.
49.75	-4.0004	-1.1761
49.85	-1.7564	-0.6219
49.95	-0.3253	-0.1828
50	-0.0318	-0.0317
50.05	-0.0507	0.0835
50.15	-1.0863	-0.1378
50.25	-3.1274	-0.1526

Table VI- THD measurement result-frequency test

References

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