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No-clean flux residues detection with impedance measurements

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***Abstract* – The no-clean flux-residues pose a high reliability risk, thus controlled strictly in the modern electronics assembly industry. A series of customized Surface Insulation Resistance (SIR) Experiments and AC impedance analysis under various test patterns demonstrate the dramatic impact of the partial activation of the fluxes unevaporated solvents, and non-decomposed activators on the reliability of the final assembly. Although the mainstream no-clean pastes and liquid fluxes are qualified under all the standard SIR and electrochemical migration (ECM) reliability tests, the solder mask filled SIR patterns are more realistic and the tests results more accurate. The spaces are filled with solder mask thus the ionic migration analysis is more complex. From this perspective, we demonstrate a thorough examination of these more realistic structures with classic DC SIR method and AC impedance measurements. This study examined the impact of no-clean flux residues on capacitance and resistance in case of solder mask filled comb patterns.**

Keywords – no-clean flux, impedance, reliability, analysis, contamination.

I. INTRODUCTION

The electronics assembly industry shows continuous development. The most important values are meeting the ever-increasing demands for miniaturization and robustness, and finally, reliability. The product cleanliness and the minimization of pollutants during production are crucial for the lifetime of the assembly. Nowadays, the use of no-clean fluxes is commonplace in soldering technology, as it has both environmental protection and cost-effectiveness advantages, and cleaning after soldering is not necessary in principle. Although the weak organic acids (WOAs) in the flux can promote ion migration and, in critical cases, a short can form, which may cause malfunction. Detection and minimization of ionic residues is crucial, therefore understanding the behaviour of impure fluxes on printed circuit boards is a cutting-edge research problem in manufacturing technology. The frequency of failures caused by ionic residues increases due to a humid and warm environment, therefore the standard investigation is usually performed in a climate chamber on normal – not solder mask coated – FR4 based test boards. The commonly applied solder mask layer on the surface of the boards modifies the morphology and electric behaviour of spaces between the electrodes, so the impedance analysis of this type of test board is useful to understand the realistic systems.

Impedance spectroscopy (IS) is a powerful characterization technique used to study the electrical (impedance/dielectric) properties of a wide variety of printed circuit boards surfaces. For bulk systems, a parallel-plate (interdigital) electrode geometry, shown in Fig. 1, is commonly used to apply a small sinusoidal voltage to the sample. The impedance of the sample (both resistive and reactive contributions) is measured over a range of frequencies, typically from 20 Hz to 1 MHz. The advantage of IS over static frequency techniques is that for a complicated system, individual components can be separated and characterized according to their different relaxation times/frequencies.

The application of interdigital structures is useful to measure the surface impedance of boards.

II. RELATED RESULTS IN THE LITERATURE

Verdignovas et al. [1] performed SIR tests and AC measurements with various weak organic acids and established that a correlation can be observed between the hygroscopic properties of residues and the water layer that forms. During climate tests, the probability of failures increases with WOA quantities and with the effect of a humid and warm environment.

Piotrowska and Ambat [2] examined residue-assisted water layer formation under transient climatic conditions with AC and DC electrochemical measurements.

Tolla et al. [3] pointed out that the complex SMD components behave differently from the standard FR4 test patterns in terms of ion migration, so they performed special SIR tests where the test panel was equipped with patterns corresponding to SMD components. Mainstream no-clean pastes and liquid fluxes, which are qualified under all the standard SIR and ECM reliability tests, present SIR values several decades lower than the 100MΩ limit mandated by IPC J-STD-004B when tested under that QFN.

Zou et al. [4] studied the low frequency AC impedance technique, which can be used as an alternative to the SIR technique.

III. DESCRIPTION OF THE METHOD

Test Boards

The measurements were performed on the SIR pattern with immersion tin (ImSn) finish, on the FR-4 test board. The size and thickness of the board were 159.5 mm × 116.8 mm and 1.6 mm, respectively. The dimensions of the SIR patterns used for leakage current measurements were the following size: 20 mm × 41.2 mm, and the spacing size was 0.73 mm for the 'big comb' (Fig. 1a) and 4 mm × 8.5 mm and spacing size was 0.15 mm for 'small comb' (Fig. 1b.). The nominal square count calculated for SIR pattern of the current dimensions are 1232.88 for 'big comb' and 720 for 'small comb'. The test board for impedance measurements was the same as for SIR tests. The spacing between opposing conduction lines (copper-defined pads) were covered by solder mask. The base material of the conducting lines was copper (~35 μm) and a top layer of tin (~1.5 μm). Prior to the application of WOAs, the test boards were brand new, in original packaging. The boards were pre-contaminated with the no-clean flux (solid content 3.3 ± 0.3%). The volume of the droplet was confined to the surface area of the test coupons, resulting in 0.178 ml/cm^2 of flux. A set of pre-contaminated test boards was also exposed to heat treatment at 140°C for 120 seconds to simulate the temperature profile likely to be experienced upon preheating and activation before the soldering process.

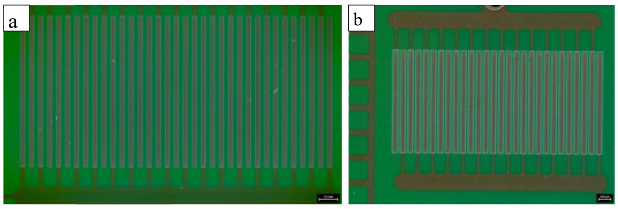

Fig. 1. 'big comb' was 20 mm × 41.2 mm, and the spacing size were 0.73 mm (a) and 'small comb' was 4 mm × 8.5 mm spacing size were 0.15 mm (b).

		Reference					Test										
Boards ImSn finish, 2 patterns		S2	S1	S1	S2	S2	S1						S2				
		7 (X)	8 (00)	7 (0)	2 (0)	6	1	2	3	4	5	6	1	3	4	5	8
Phase 1 (original)		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
Fluxing		-	-	-	-	-	+	+	+	+	+	+	+	+	+	+	+
Phase 2 (after fluxing)		-	-	-	+	+	+	+	+	+	+	+	+	+	+	+	+
Preheat		-	+	-	+	+	-	-	-	+	+	+	+	+	+	+	+
Phase 3 (after preheat)		-	+	-	+	+	-	-	-	+	+	+	+	+	+	+	+
SIR 40°C 90% RH 10V	0V (Condition)	-	+	+	-	-	+	+	+	+	+	+	-	-	-	-	-
	10V (Condition)	-	-	-	+	+	-	-	-	-	-	-	+	+	+	+	+
Phase 4 (End of experiment)		+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

Fig. 2. Example of an experimental design table.

Electrochemical Measurements

In our work three independent measurements were used to study of the PCBs:

1) Electrochemical measurements were performed by using an AD5934 Impedance Converter IC. In case of Series 1 the impedance measurements were performed on 'small comb' at a frequency of 5kHz. All two patterns were investigated by this method in the Series 2.

2) The Agilent 4284A precision LCR meter collected the capacitance spectra with AC signal with amplitude of 2V from 20Hz to 1MHz by C_P-R_P equivalent circuit model. The channels of the instrument were connected in a two-electrode cell configuration. The spectral data were collected on both patterns in each experiment phase.

3) The leakage current was measured on SIR patterns pre-contaminated with flux and exposed to humidity inside a climatic chamber. The humidity was at 90%RH, while the temperature was kept constant at 40°C throughout the experiment. The current was measured as a function of the applied potential, which was 10 V. The measurements were performed for 1 week. In case of Series 2 the parameters were same except that the 10 V condition potential was applied under the whole test. The local ionic contamination of the surface can be easily specified by the Corrosivity Index (CI) which is a destructive, non-repeatable test.

Microscopy

The boards were observed by Leica DVM6 A video microscope and FEI Inspect S scanning electron microscope (SEM) after the test. The elemental analysis of patterns was performed by EDAX Octane Elite EDS system with Octane Elite silicon drift detectors (SDDs).

The experimental design table presented in Fig. 2. and the flowchart of the experiment in Fig. 3.

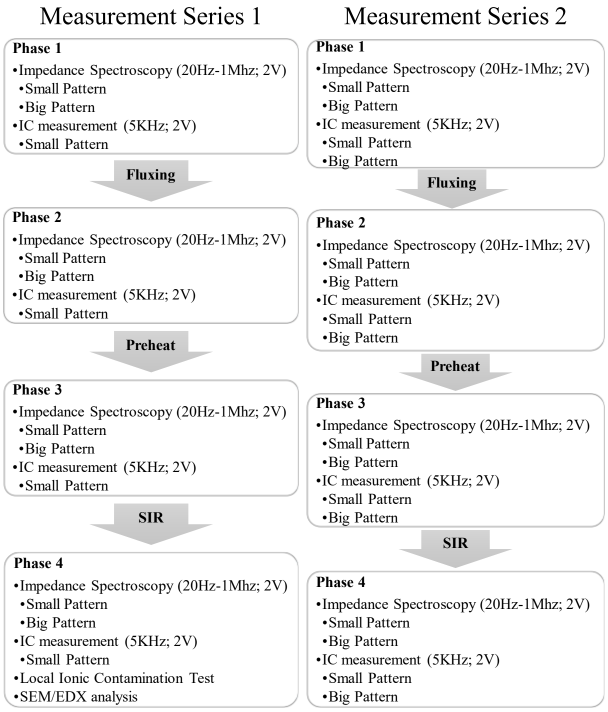

Fig. 3. Flowchart of experiments

IV. RESULTS AND DISCUSSIONS

The experiment was performed in 4 different phases on 6 boards in case of Series 1, and 5 boards in case of Series 2. All boards were measured with all electrochemical methods. The measured impedance, capacitance and resistance values were normalized with the Phase 1 (original) reference values to compensate for the effect of environmental factors and variation of boards.

Based on the statistical examination of the boards, no change was observed in the measured capacitance values of reference samples during the entire duration of the experiment. In addition to constant temperature and humidity, there was no significant time dependence in the tested values. The value of the measured impedances is determined by the properties of the individual boards in their original state. The standard deviation between the test samples is also determined by the differences in the individual values of patterns.

Based on the repeatability and reproducibility tests, the standard deviation of each tested original sample compared to the time is less than 1%, therefore the individual experimental phases can be well characterized by the average of the capacitance or resistance values of the test patterns.

In the case of flux-treated boards (Phase 2), the variance due to the uncertainty of the contamination dosage is also not negligible, but even in this case, the variances between the samples are minimal compared to the extent of the changes between the phases.

During gravimetric tests, a straight-line relationship was demonstrated between the mass of the dry residue applied to the surface and the volume of the liquid flux. In addition, a correlation can be established in the tested range between the results of the two types of capacitance and impedance measurements at the same AC voltage and frequency.

The pollutant had the same material composition in case of both series, but the applied no-clean flux had a significantly different mixing ratio between Series 1 and 2. This can be observed in the intensity normalized capacitance of changes between phases as well.

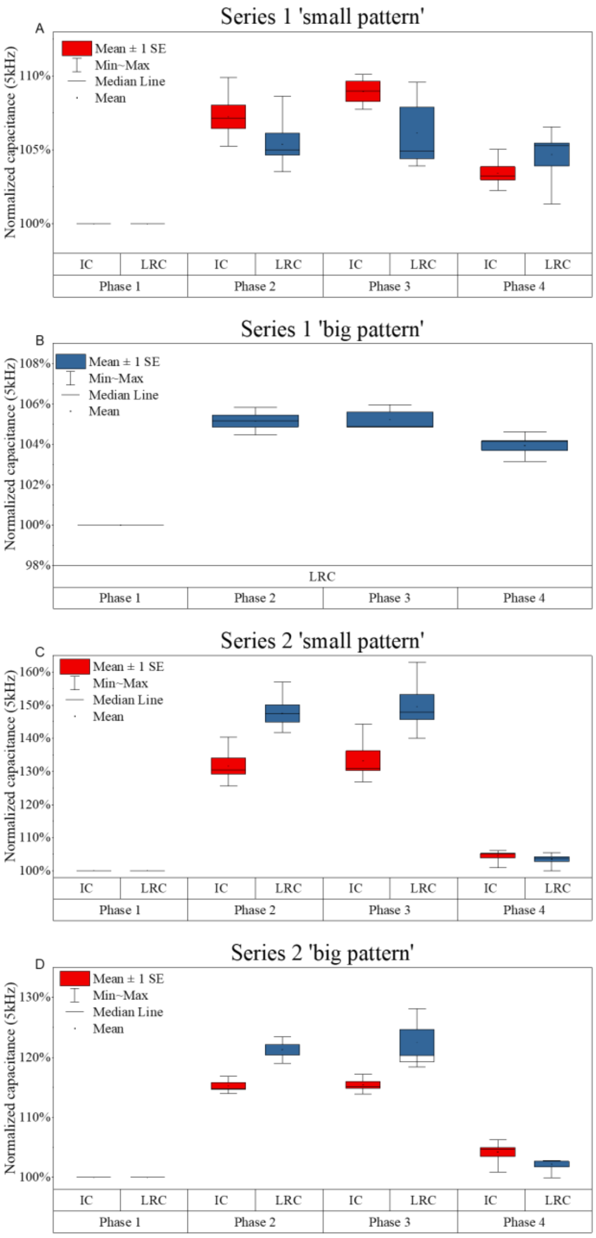

Fig. 4. The normalized average capacitances of patterns (100%: average of original boards capacitance value)

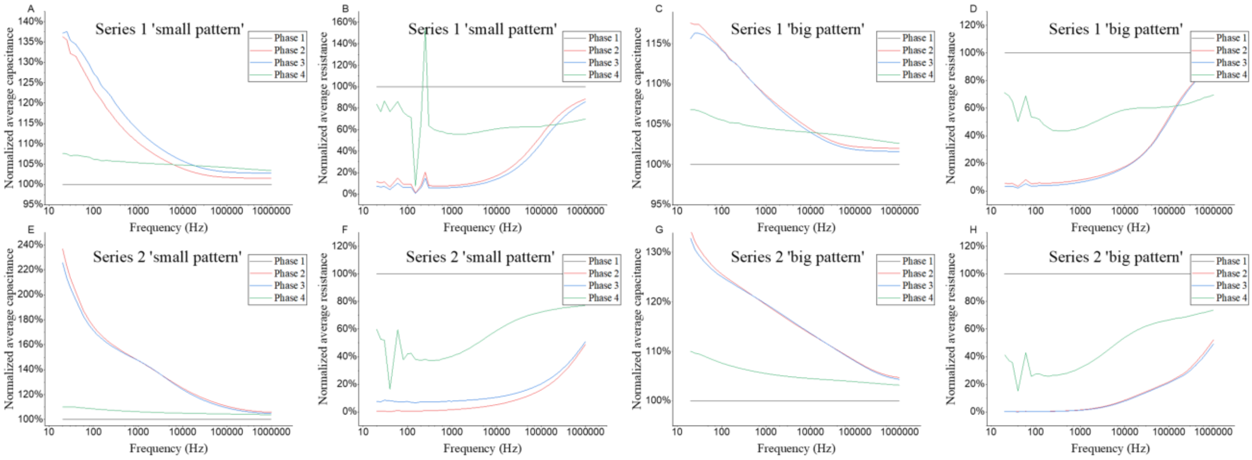

Fig. 5. Impedance (capacitance, resistance) spectra of samples.

The effect of flux residue (Phase 2) is detectable based on the increase of measured capacitances (Fig. 4.). The heat-treated (Phase 3) measurements present similar values. After the SIR and storage tests (Phase 4) the capacitance decreased, therefore the values do not fall under the reference value. The converter IC method and the LRC method results show good agreement at 5kHz frequency. The behaviour of the patterns were consequential in each Phase.

The impedance spectroscopy measurements were performed in both patterns. All patterns show similar properties, as it is presented in Fig. 5. The measured resistance is decreasing, and the capacitance is increasing at low frequencies due to flux residues (Phase 2). The electrical properties of the surfaces change as well. The measurements after the SIR and storage show normalization, although the moisture and the condensed water propagated the distribution of flux. The probability of ionic migration increased, and the traces of residue were detected by impedance analysis in Phase 4 as well.

The flux contamination does not change the electronic properties so radically at high frequencies, which is in agreement with the research of Jennifer Nguyen[5].

The SIR test (Fig. 5). was performed after Phase 3. Most of the flux-contaminated patterns did not reach 100MΩ surface resistance in the first 12 hours. A moderate rise was observed in all cases although this tendency stopped after a few days. The resistances of test samples stabilized at 10^8-10^9 Ohm and did not reach the surface insulation resistance of reference samples. No significant differences were observed in Series 1 and Series 2 test results. During the SIR test, the effect of the 10 V conditioning potential was not detectable in the case of Series 2.

The microscopic inspection after the SIR test presents white residues on the flux-contaminated regions. The residue does not spread evenly on the surface, but rather aggregates at the edges of the tin fingers. In some cases, the white residues interconnect two conductive fingers or violate the minimum electrical clearance.

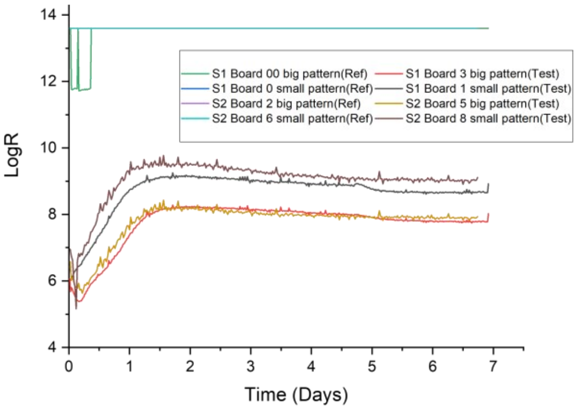

Fig. 6. SIR test results 40°C 90RH% 10V (examples).

After the experiment visual investigation was performed and the ionic contamination levels were determined by the destructive C3/C.I. method. The reference patterns were ‘clean’ and all contaminated patterns were extremely ‘dirty’ (Fig. 7.).

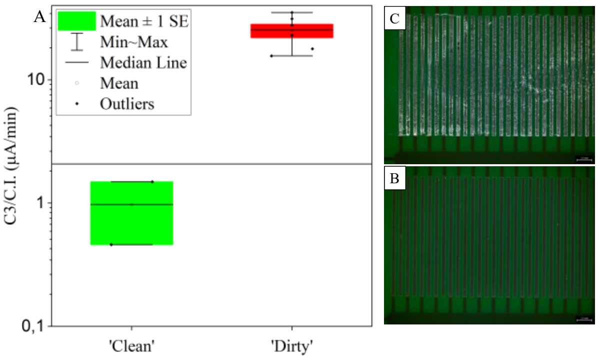

Fig. 7. ‘Big comb’ cleanliness test results (A). Optical microscopy images of reference (B) and flux-contaminated (C) pattern after the experiment.

Based on SEM images the ion migration was evident, however dendrites were not observed on the solder mask strip. Some minor dendrites were visible in the gap near the tin-rich electrode and increased amount of flux residues can be seen near the other side. The line analysis of Energy Dispersive Spectroscopy proves that the thickness distribution of the surface tin coating has changed between electrodes with different potentials.

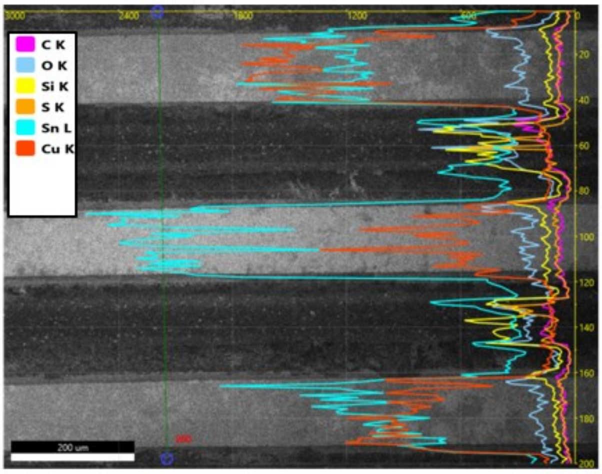

Fig. 8 'Small comb' SEM BSE image after the experiment, and EDX line analysis.

V. CONCLUSIONS AND OUTLOOK

1) Electrochemical testing of ethanol base WOAs (OR/L0) used as part of no-clean flux systems showed a clear correlation between the residues and the impedance values. After the climate tests and storage, flux residues were detected by ionic contamination measurement, visually and via impedance tests.

2) After applying no clean flux, a measurable change in the capacitance of all contaminated patterns were observed, which may be caused by WOA residues accumulated in the gaps of the copper-defined pads.

3) By analysing the impedance spectra, a significant increase in capacitance is demonstrated and a decrease in resistance were detected at low frequencies.

The freshly dried samples show similar behaviour as the samples in the heat-treated phase due to partially activated flux residues. For higher frequencies, the effect was less significant.

4) The SIR test and SEM-EDX results indicate that tin migration occurred during the climate test, but there was no typical formation of dendrites on the solder mask surface between the conductive surfaces.

5) Overall, the results show that the residues of the WOAs used in no-clean fluxes can affect the electronic properties of board surfaces. Therefore, minimalization of the flux usage might be important [6] or post-cleaning methods [7] should be applied when electronics need to operate under safety-critical conditions.

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