2011 International Workshop on ADC Modelling, Testing and Data Converter Analysis and Design and IEEE 2011 ADC Forum
June 30 - July 1, 2011. Orvieto, Italy.

Testing the Transmission Path of a Software Defined Radio Platform

Chiara Maria De Dominicis[1], Luca De Vito[2], Paolo Ferrari[1],
Alessandra Flammini[1], Sergio Rapuano[2]

[1] *Department of Information Engineering, University of Brescia, Brescia, Italy*
{chiara.dedominicis, pferrari, flammini}@ing.unibs.it
[2] *Department of Engineering, University of Sannio, Benevento, Italy*
{devito, rapuano}@unisannio.it

Abstract *- The paper presents the experimental characterization of the transmission path of a Software Defined Radio (SDR) platform. The characterization has been conducted by determining the standard parameters for the digital-to-analog converter testing in the frequency domain. In particular, a test method using sinewave input signals and a spectrum analyzer has been used. Experimental results have been conducted by using two different signal generation configurations offered by the SDR platform. In the former, the signal generation is realized by software in the computer connected to the SDR; in the latter, the signal generation task is left to the numerically controlled oscillator located in the SDR CODEC.*

I. Introduction

In last years, the trend of electronics goes quickly towards the integration of multiple circuits into Systems-On-Chip (SoCs). Such systems often bring together not only analog and digital subsystems, but also radio frequency (RF) components allowing wide-bandwidth communication, optics and microelectromechanical systems (MEMS) as interfaces with the outer world [1]. Several applications require the integration of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) into compact mixed-signal SoCs.
Standard test methods are often hard to apply to ADCs and DACs, which are integrated in SoCs, due to the unavailability of input or outputs directly connected to the device under test, and to the multiple configurations of the other digital or analog circuits integrated in the same chip with the device under test.
Among the SoCs, containing A/D and D/A sections, the Software Defined Radio (SDR) systems are gaining a noticeable interest, as they represent the hardware platform for new generation telecommunication equipment. These systems are based on minimal hardware components and rely on software for all communication functions, such as modulation/demodulation, source and channel coding/decoding, and so on. Therefore, the ADC and DAC will play a greater role in determining the performance of the whole communication system than in traditional circuits for telecommunication applications [2],[3].
In [4], the authors analyzed the feasibility of adopting standard parameters and test methods to characterize the SDR receiving path. In particular, it has been observed that several problems should be faced during the SDR A/D conversion testing, due to the presence of other circuits and the unavailability of the codes just after the A/D conversion.
In this work, a similar approach has been followed to evaluate the possibility of using standard parameters and test methods [5],[6],[7], to characterize the SDR transmission path in the frequency domain. To this aim the considered parameters and test method comply to the upcoming IEEE P1658 “Draft standard for terminology and test methods for digital-to-analog converters” [8].
In particular, attention have been paid to the selection of the point of the transmission chain where the test signal is generated. Since the SDR realizes the digital upconversion, as shown in Fig.1, sinewave signals for the dynamic characterization of the D/A section can be generated either by the software in the microprocessor connected to the SDR, or by the Numerically Controlled Oscillator (NCO), located in the digital circuits of the SDR. These two modes of signal generation can lead to different results, due to the activation of different digital circuits which are present in the two paths.
In Section II, the SDR platform used in this work will be briefly described. In Section III, the parameters and test methods used in the test phase are presented. In Section IV, the experimental results are reported and discussed.

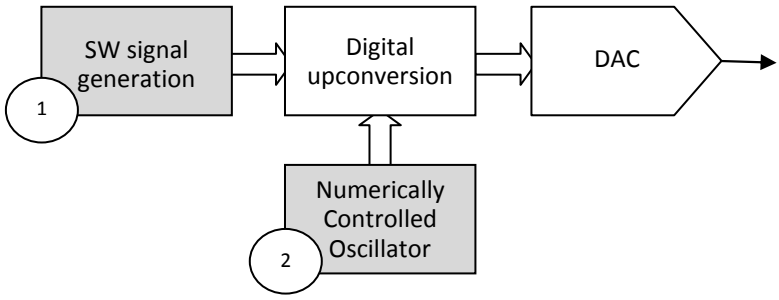

Fig.1. In a SDR, since a digital upconversion is realized, sinewave signals can be generated either by the software in the microprocessor connected to the SDR (1), or in the NCO located in the SDR digital circuits (2).

II. The SDR platform

An open source project called GNU Radio has been chosen for the realization of the developed test bench. GNU Radio architecture is composed by a minimal hardware and a modular, expandable and block-organized software library developed by GNU Radio community. The software side of the GNU Radio is based on Linux Operating System, C++ compiler and Python interpreter. Several different radio frequency frontends may be used with GNU Radio, but the mostly used one is the Universal Software Radio Peripheral (USRP). The USRP well matches the need to interface a general purpose PC to the radio frequency world in a low-cost and high-speed way.
The USRP motherboard hosts a CODEC, with two 12-bit ADCs (64 MS/s sampling rate) and two 14-bit DACs (128 MS/s), and an Altera FPGA for simple high speed operations as up-conversion, down-conversion, interpolation and decimation. ADCs and DACs allow to receive baseband signals up to 32MHz and to generate baseband signals up to 50MHz. Several Radio Frequency analog boards may complete the USRP hardware.
Attention is focused here on the transmission path, where the processing of the samples is divided between the FPGA and the CODEC which hosts the stage of D/A conversion, as shown in Fig.2. The complex samples generated by software, suitably interlaced in in-phase and quadrature (I/Q) parts are then packetized and transferred by means of USB (FX2); finally, they are placed in the FIFO buffer inside the FPGA. A subsequent de-interleave block performs demultiplexing of data separating flows into I/Q streams according to the number of channels to be transmitted.
Each pair of I/Q samples enters into a module which interpolates data to the fixed rate of 32MS/s using CIC (Cascaded Interpolated Comb) filters; it is worth to note that CIC filters, implemented within the FPGA, can be considered as the first stage of the Digital Up Converter (DUC). The outputs of the interpolation stage are connected to de-muxes, allowing setup the routing of data; samples are then reduced from 16 to 14 bits, by eliminating the two least significant bits, in order to match the data bit size of the DACs in the CODEC.
At this point, the samples enter the CODEC that implements the remaining part of the DUC by means of a fine complex multiplier, an half band filter, and finally a coarse complex multiplier: I and Q data are first shifted in frequency, then interpolated by a factor of 4 by means of the filter and, finally, frequency-shifted again. At the end of the chain, the data stream at 128MS/s is converted by the DAC.
It is possible to identify, in the scheme of Fig.2, the two generation paths of the sinewave test signals. The former starts with the generation of the I and Q samples in the PC, going through the FPGA and the CODEC towards the DAC; the latter starts with the generation of the samples in the NCO, located in the CODEC, and proceeds through the DUC, towards the DAC.

III. Parameters and test methods

Since static and dynamic non-linearities will show up in the frequency domain contributing to the DAC distortion performance, a high speed DAC should be primarily evaluated using specifications and characterization data pertaining to frequency domain [9].
One of the most quoted DAC specification in the frequency domain is the Spurious-Free Dynamic Range (SFDR), which is directly affected by the main distortion component. It is defined as the amplitude distance between the amplitude of the fundamental(s) and the amplitude of the largest non-fundamental (spurious) component in the frequency band of interest [8].

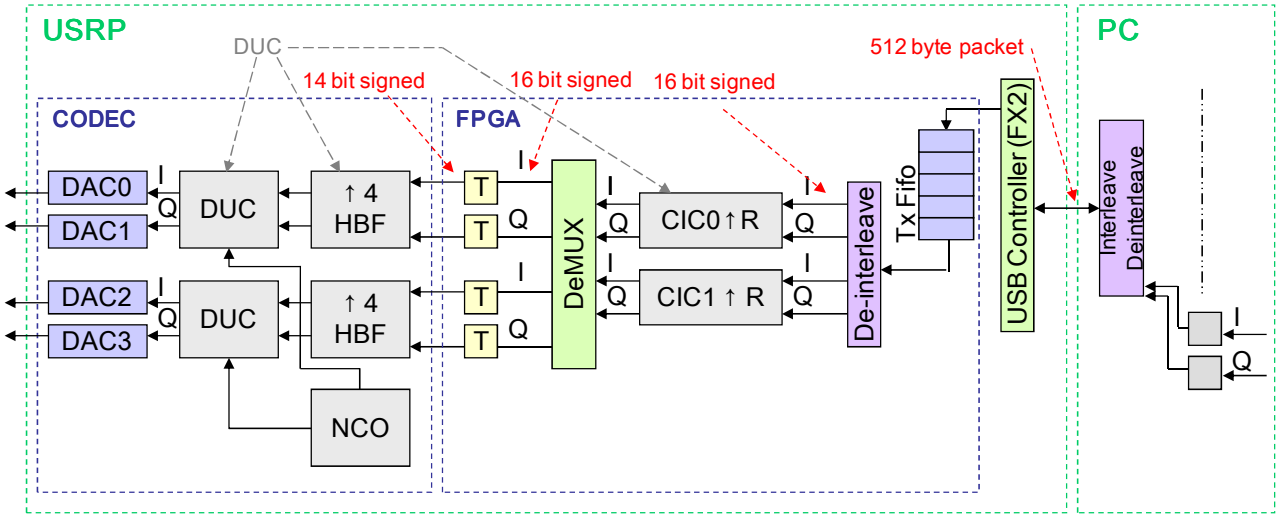

Fig.2. Block diagram of the transmission path in the GNU radio platform.

The noise performance of a DAC is also important in determining a DAC's suitability in various communication applications (i.e. spread spectrum). In these applications, the Carrier-to-Noise Ratio (CNR) of the reconstructed waveform, which includes the effects of both noise and distortion, will directly affect the bit error rate (BER) of the system [9]. In order to measure the noise performance of the DAC, two parameters are mainly used, either including or excluding distortion. They are the SIgnal-to-Noise And Distortion ratio (SINAD) and the Signal-to-Noise Ratio (SNR). The former is defined as the ratio of the root-mean-square (rms) signal to the rms noise and distortion for sinewave output signals. The latter, defined as the ratio of rms signal to rms error of the least squares sinewave fit can be also seen as the same as SINAD excluding the harmonic distortion energy [10].
As specified in [8], in order to perform the DAC dynamic test in the frequency domain, a digital sinewave signal should be applied as input, while the analog DAC output should be observed by means of a spectrum analyzer or by a high resolution base band data acquisition system. However, for telecommunication applications, it is difficult to find baseband high resolution sampling instruments, since the required sampling frequency is very high. For this reason, it has been preferred to use a spectrum analyzer, connected to the USRP as shown in Fig.3.
Both SFDR and SINAD have been obtained in the frequency domain, starting from the spectra acquired by the spectrum analyzer. The spectra have been first processed to obtain an estimate of the following quantities:

- the power of the signal component;
- the power of the main harmonic or spurious component;
- the power of the noise.

The power of the signal component has been obtained by identifying from the acquired spectrum the lobe B_1 corresponding to the convolution of the highest spectral component with the Fourier transform of the spectral window. To this aim, the frequency bin containing the highest value of the spectrum is found and the nearest local minima are searched at both sides of such bin. The positions of the local minima identify the boundaries of the lobe B_1, as shown in Fig.4.
Then, the power of the main component is evaluated by taking the integral of the signal power in the mainlobe, and correcting by the Noise BandWidth (NBW) of the spectrum analyzer window:

Fig.3. Test bench for dynamic testing of the SDR transmission path in the frequency domain.

$$P_1 = \sum_{k=k_1}^{k_2} 10^{\frac{S(k)}{10}} \cdot \frac{\Delta f}{NBW}, \tag{1}$$

where, *S(k)* is the k-th bin of the acquired spectrum, *Δf* is the frequency resolution, that is the frequency span divided by the total numbers of bins, k_1 and k_2 are the bins corresponding to the boundaries of B_1.
The NBW of the spectrum analyzer window is the bandwidth of an ideal filter having a constant passband gain which passes the same rms noise voltage, where the input signal is white noise [11] and it is defined by the following formula:

$$NBW = \frac{1}{A_{v0}^{\ 2}} \int_0^{\infty} \left| A_v(f) \right|^2 df, \tag{2}$$

where, $A_v(f)$ is the frequency response of the window and A_{v0} is the maximum value of $A_v(f)$.
In a similar way, the second highest value of the acquired spectrum is evaluated. It allows identifying the lobe B_h, which is produced by the convolution of the highest spurious or distortion component with the Fourier transform of the spectral window. As in the previous case, B_h is identified starting from the highest value and searching for the nearest local minima. The power of the highest spurious or distortion component is obtained by integrating the power under the lobe B_h and correcting by the NBW:

$$P_h = \sum_{k=k_3}^{k_4} 10^{\frac{S(k)}{10}} \cdot \frac{\Delta f}{NBW}, \tag{3}$$

where, k_3 and k_4 are the bins corresponding to the boundaries of the lobe B_h.
Instead, the noise power is evaluated by integrating the acquired spectrum in the whole frequency span, with the exception of the lobe B_1. Then, the integral is corrected by the NBW and expanded by assuming that a contribution of noise is present inside the lobe B_1, too, with a power density equal to the mean power density observed in the rest of the frequency span:

$$P_n = \frac{N_r}{N} \sum_{k \notin B_1} 10^{\frac{S(k)}{10}} \cdot \frac{\Delta f}{NBW}, \tag{4}$$

where, N_r is the number of bins in the integrating band and N is the total number of bins in the whole span.
Once evaluated the powers of the main component, of the highest harmonic or spurious and of the noise, it is possible to obtain both the SFDR and the SINAD, from the following expressions:

$$SFDR = 10 \log_{10} \frac{P_1}{P_h}, \tag{5}$$

$$SINAD = 10 \log_{10} \frac{P_1}{P_n}. \tag{6}$$

The values obtained by (5) and (6) are collected as results of the characterization.

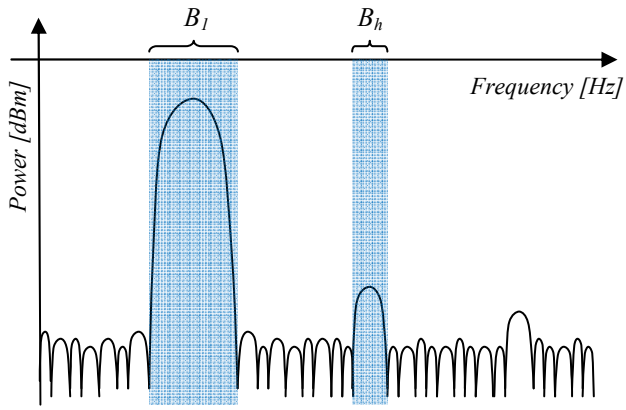

Fig.4. Graph of a generic spectrum, in which the lobes B_1 and B_h are identified by marking the highest peak and the second highest peak and searching the nearest minima.

Due to missing details, in the current version of the IEEE P1658 Draft Standard [8], about measurements of DAC dynamic parameters in the frequency domain by means of a spectrum analyzer, the proposed processing approach could be adequately included in a future revision of [8].

IV. Experimental results

As described in Section I, in a SDR, several modes can be used for the generation of the test signals. In particular, they can be created with three different methods: (i) they can be generated by the PC software and sent transparently to the DAC; (ii) they be created by the FPGA/ASIC alone and sent to the DAC; and (iii) they can be the result of a PC signal mixed with a USRP generated signal.
The performance of the digital-to-analog section of the SDR has been characterized in terms of SFDR and SINAD, in the first two cases.
Results have been reported in Fig. 5 for the quadrature channel. Similar results have been observed for the in-phase channel. In particular, Fig. 5a and Fig. 5c refer to the tests with software generated signals. Instead, Fig. 5b and Fig. 5d refer to tests using the FPGA/ASIC generation.
As it can be seen, a similar behaviour on both cases has been observed for the SFDR, where best results have been obtained with higher frequencies and amplitudes close to the full scale. This is explained by observing that with higher frequencies, the third harmonic, which is the spectral component determining the SFDR goes outside the band of the DAC interpolating filter. In this case noise and spuria determine the SFDR, thus the SFDR increases with the amplitude. With lower frequencies, the SFDR is quite constant versus the amplitude of the test signal to about 70dB.
SINAD has in all cases an increasing behaviour with the amplitude, thus it seems it is dominated by noise and spuria, which do not depend on the amplitude of the test signal. For a test frequency equal to 1MHz, slightly lower values have been observed for the software generated signals than for the hardware generated ones. This may be due to the additional interpolating filter (CIC) and half band filter, placed between the sample generation and the digital mixing, that are activated when the test waveform is software generated.

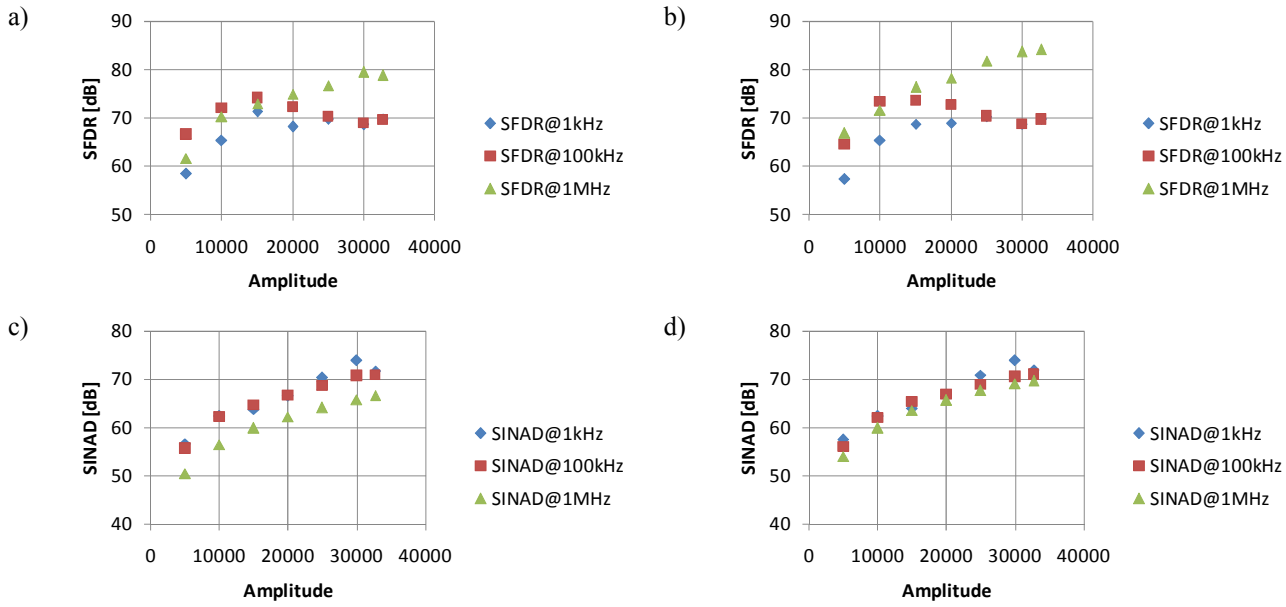

Fig. 5. Experimental results of the characterization of the SDR transmission path. SFDR (a and b) and SINAD (c and d) values in the case of sinewave signal generated by the PC software (a and c) and in the case of sinewave signal generated by the USRP hardware alone (b and d).

V. Conclusions

In this paper, the characterization of the transmission path of a SDR platform has been carried out, by determining the standard parameters for dynamic testing of DACs in the frequency domain. In particular, a test method using sinewave inputs and a spectrum analyzer has been used. The spectrum analyzer traces have been then processed to obtain an estimation of the parameters. The proposed processing approach could be adequately included in a future revision of the "IEEE P1658 Draft Standard for terminology and test methods for digital-to-analog converters" [8].
Tests have been conducted by applying the sinewave signals in two configurations, whether the samples of the waveform are generated by software or the SDR is instructed to generated samples by its hardware. Experimental results show in general a good agreement between the two configurations, with slightly better results for SINAD in the

case of hardware generated signals. Further work is directed to the characterization of the SDR in terms of other parameters, even involving multiple frequency signals, such as Total Harmonic Distortion and Intermodulation Distortion. In addition, further research will be directed to experimentally evaluate the relation between the digital-to-analog section parameters and the quality of the transmitted signal.

Acknowledgements

The authors would like to thank Prof. Pasquale Daponte for his useful suggestions during all the phases of this research work.
The research has been funded by the Italian Ministry of Education, University and Research within the project "A/D and D/A conversion metrology: standardization of the figures of merit, error estimation and correction, uncertainty evaluation", PRIN 2008, prot. 2008S9J8XE.

References

[1] S.S.Akbay, A.Halder, A.Chatterjee, D.Keezer, "Low-cost test of embedded RF/analog/mixed-signal circuits in SOPs", IEEE Trans. on Advanced Packaging, vol.27, No.2, May 2004, pp.352-363.
[2] R.H.Walden, "Analog-to-digital converter survey and analysis", IEEE Journal on Sel. Areas in Telecomm., vol.17-4, April 1999, pp.539-550.
[3] T.Araújo, R.Dinis, "Analytical evaluation and optimization of the analog-to-digital converter in software radio architectures", IEEE Trans. on Vehic. Tech., vol.56, No.4, July 2007, pp.1964-1970.
[4] P.Daponte, L.De Vito, S.Rapuano, C.M.De Dominicis, P.Ferrari, A.Flammini, "Characterization of the A/D conversion section in Software Defined Radios", Proc. of IEEE Int. Instrum. and Meas. Tech. Conf. (I^2MTC), May 2010, pp.357-362.
[5] E.Balestrieri, P.Daponte, S.Rapuano, "Recent developments on DAC modelling, testing and standardization". Measurement, vol.39, No.3, Apr. 2006, pp.258-266.
[6] E.Balestrieri, S.Rapuano, "DAC consistent terminology: static parameter definitions", Measurement, vol. 40, No.5, June 2007, pp.500-508.
[7] E.Balestrieri, "DAC Time-Domain Specifications Toward Standardization", IEEE Transactions on Instrumentation and Measurement, vol. 57, No.7, July 2008, pp.1290-1297.
[8] IEEE, "IEEE P1658 draft standard for terminology and test methods for digital-to-analog converters", Oct. 2010.
[9] W.Tuttlebee, "Software defined radio: enabling technologies", John Wiley & Sons, 2002.
[10] E.Balestrieri, S.Rapuano, "Defining DAC performance in the frequency domain", Measurement, vol. 40, No, 5, June 2007, pp.463-472.
[11] J.G.Webster, "The measurement, instrumentation, and sensors Handbook", CRC Press, 1999.