13th Workshop on ADC Modelling and Testing
Sep. 22-24, 2008, Florence, Italy

ADC Peripheral in Microcontrollers

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Abstract- This paper presents an analog-to-digital converter (ADC) embedded as a peripheral in a microcontroller and influence of asynchronous digital input signals on results of ADC conversion. A schematic diagram of a SAR ADC peripheral analog input circuit in a microcontroller was described and its model was designed. A practical measurement was performed using crosstalk measurement setup and causes of measurement errors were identified.

I. Introduction

A microcontroller can be found in embedded systems where it very often interfaces analog and digital world by means of and analog-to-digital converter (ADC). Its function can be to measure an analog signal, process data and show results in case of an embedded measurement system. The ADC embedded as a peripheral in the microcontroller can be used for measuring the analog input signal. The ADC can be of various architectures. A successive-approximation-register ADC (SAR ADC) is a typical architecture of the ADC embedded as a peripheral in microcontrollers. An 8-bit, 10-bit or 12-bit SAR ADC with a conversion time about 2 µs and multiplexed inputs is usually available in microcontrollers. Also 16-bit or 24-bit ADCs are available (not SAR architecture, very often the sigma-delta architecture) but a long conversion time of these high-resolutions ADCs is only usable for DC signal measurement.
There are many microcontroller manufacturers on the market; however, they offer very similar designs of their microcontrollers. The design is limited by a microcontroller package pin count; it leads to a situation when one pin is shared by two or even more peripherals and also both digital and analog power supply is sometimes be shared. Basic peripherals are counters, timers, and digital input/output. These peripherals allow the microcontroller to control other components in the embedded system and enable measurements of digital signals (i.e. periodical time measurement). The microcontrollers with the ADC peripheral are mixed-signal systems-on-chip (SoC) and in this paper it is shown that some digital switching noise can affects the ADC conversion results. This noise is measured and it is made a recommendation to reduce it. The inspiration comes from reference [1], [2], where the authors described digital switching noise.

II. SAR ADC peripheral and microcontroller

Analog-to-digital converters also, of course, exist as standalone integrated circuits and with those embedded as peripherals in microcontrollers they have some common features. These features are independent on the manufacture – an analog input circuit and a timing of SAR ADC, for instance.

A. SAR ADC analog input circuit

A typical schematic diagram of a SAR ADC peripheral analog input circuit in a microcontroller is shown in Figure 1. This schematic diagram was obtained from datasheet [3] and modified by information from datasheet [4]. The value of voltage V_{ADC} is $V_{DD}/2$ in case of an Atmel microcontroller [4].
The typical value of the pin capacitance C_{PIN} is about 5 pF. The other parameters are very dependent on a manufacturer. The serial resistance can vary in the range from 1 kΩ to 100 kΩ in an Atmel microcontroller [4]. The value of sampling capacitance C_{ADC} is 120 pF in a PIC microcontroller [3] or it is 14 pF in an Atmel microcontroller [4]. This capacitance is only connected to the input pin when a SAR ADC is sampling. The values of SAR ADC peripheral analog input circuit in a PIC microcontroller [3] are shown in Table 1.

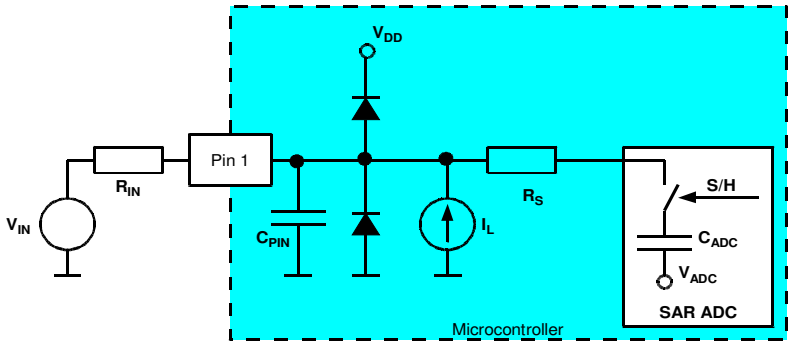

Figure 1. Schematic diagram of SAR ADC peripheral analog input circuit in a microcontroller.

Table 1. Component values of SAR ADC peripheral analog input circuit in a PIC microcontroller [3].

Symbol	Description	Typical value
V_{IN}	Input source voltage	-
R_{IN}	Input source resistance	-
C_{PIN}	Pin capacitance	5 pF
I_L	Leakage current	±500 nA
R_S	Serial resistance	8 kΩ
C_{ADC}	Sample/Hold capacitance	120 pF

B. SAR ADC timing

The converter, either standalone or embedded, has to have a clock source for timing. The timing of a SAR ADC peripheral is common for any microcontroller and it is shown in Figure 2. The SAR ADC peripheral is clocked by ADC_{CLK} which should be in the range specified by the manufacturer. This clock signal is typically derived from the CPU clock signal. It is required to use internal oscillator if the CPU clock is too slow. This internal oscillator is especially devoted to the SAR ADC peripheral and cannot be used by any other peripheral. A trigger (signal ADC_{START}) is required to get the sample from a selected analog input. Triggering can be done in software (by setting a bit in register) or by other sources, like external trigger (typically clocked by ADC_{CLK}) or internal timer overflow. When the ADC_{START} signal is asserted the first rising edge of signal ADC_{CLK} starts a sampling period (or falling edge – it is depended on the architecture). During the sampling period a sampling capacitance C_{ADC} (Figure 1) is connected to the selected analog input to be charged to a value given by the input voltage. This is represented by the signal ADC_{SH}. The duration of this period can be extended to more than one period of the ADC_{CLK} clock. At the end of the sampling period the capacitance C_{ADC} is disconnected and the SAR ADC peripheral continues by a conversion. The conversion takes N cycles of ADC_{CLK} clock (N corresponds to the ADC resolution in bits). The first cycle of the conversion is used to determine MSB value, the second cycle to determine MSB-1 value and it continues down to LSB value. After finishing the conversion the SAR ADC peripheral can immediately start a new sampling period (Free Running mode) or it waits for a next trigger. This operation is more described in [4].

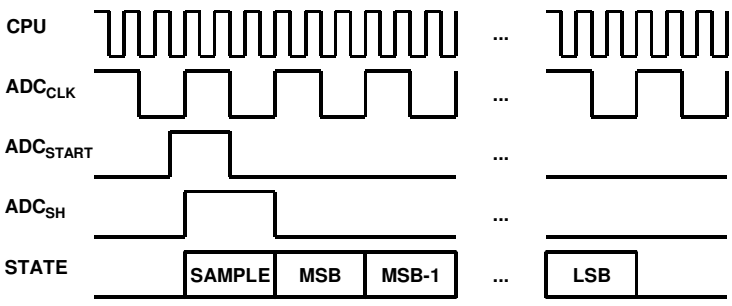

Figure 2. Typical timing of the SAR ADC peripheral circuit in a microcontroller.

III. Crosstalk measurement

Typically, a SAR ADC peripheral does not use sampling circuitry as it is expected. The capacitance of a SAR ADC structure is used as part of sampling circuit – represented in Figure 1 as the sampling capacitance C_{ADC}. Typically, no input buffer is employed in a microcontroller peripheral ADC in order to reduce input channel capacitance. In this case, the value of the analog input source resistance R_{IN} is important for a valid conversion.
Some digital (logic) signals are often present in an embedded measurement system and they are connected to the microcontroller. The digital signals can be asynchronous with respect to the internal clocking from which the ADC is also clocked. Figure 3 shows a situation where one analog signal is connected to the input channel of the SAR ADC peripheral and another digital input signal is connected to a counter peripheral. It is expected that the result of an ADC conversion can be affected by crosstalk between the digital input signal and the analog one at the end of sampling period ADC_{SH} (Figure 2).

A. Crosstalk measurement setup

The analog source V_{IN} with serial impedance R_{IN} is connected to the analog input channel labelled as pin 1 in Figure 3. The digital source V_{TLL} with serial impedance R_{TTL} is connected to the input pin labelled as pin 2 which is shared by an analog multiplexer input channel MUX and a counter peripheral. Pin 3 is configured as output port and it is generating a trigger pulse by software before a SAR ADC peripheral starts sampling. The trigger is required to synchronize internal clock of the microcontroller with clock of the digital source V_{TLL}. The MCB2100 Evaluation Board with a microcontroller LPC2129 [5] was used. The LPC2129 has a 10-bit SAR ADC peripheral.

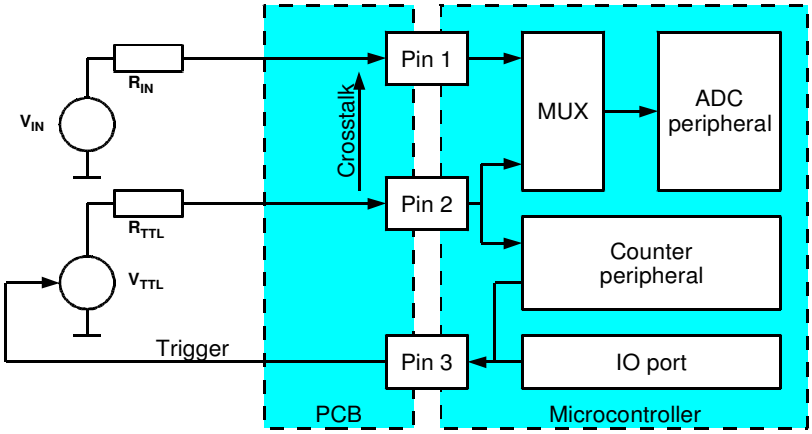

Figure 3. Crosstalk measurement setup.

B. Crosstalk measurement results

For the measurement a constant voltage V_{IN} was selected (825 mV that corresponds to the ADC result 256). The digital source V_{TTL} is a pulse generator with amplitude of 3.3 V and programmable delay, which is triggered by the microcontroller. The trigger has a jitter close to 33 ns because of the 30 MHz oscillator in the generator. The serial resistance R_{IN} of the analog source is being changed to values 50 Ω, 180 Ω, 350 Ω and 610 Ω during the experiment. The serial resistance R_{TTL} of digital source is constant and it is 50 Ω. The delay is programmable with step 2.3 ns and the zero value is selected as delay for which the crosstalk interference disappears. This should be close to the end of the sample period of the SAR ADC (see Figure 2). It can not be determined correctly because manufacturer's datasheet [5] does not contain enough information.
The measurement is carried out so that the microcontroller captures 100 000 samples and calculates the mean value. Each sample takes 11 cycles of the SAR ADC peripheral clock which has frequency 1 MHz (it was divided from CPU clock which is 60 MHz). One cycle is used for sampling period (1 µs). The results of crosstalk measurement for various serial resistances R_{IN} are shown in Figure 4 – the top figure is for a rising edge, the bottom one is for a falling edge of digital signal.

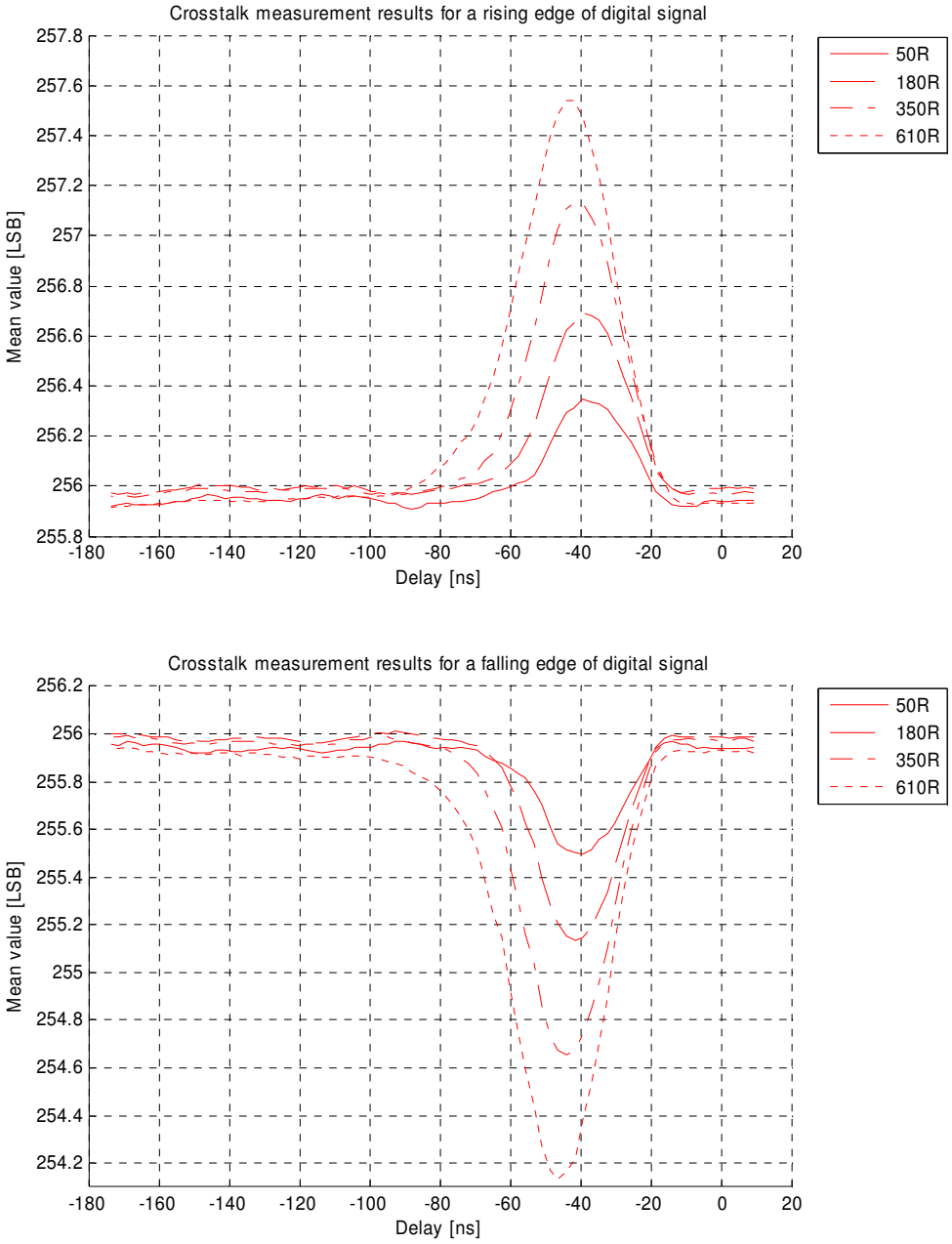

Figure 4. Crosstalk measurement for various serial resistances R_{IN}. Analog input is kept at the level corresponding to 256 LSB. Mean value is calculated from 100 000 samples. Each sample takes 11 cycles at frequency 1 MHz.

From the results, it can be concluded that if a serial resistance R_{IN} of the analog source is 610 Ω then the falling edge of digital pulse changes a conversion result nearly by 2 LSB in the worst situation. This can cause a wrong reading. It is important the time when the edge occurs.

C. Recommendation for asynchronous digital signals

As it was explained and investigated in the previous paragraphs of the paper, asynchronous digital signal, which are connected to the microcontroller during a SAR ADC operation, can affects results of SAR ADC conversion. For such situations a gate, which disables the digital signal during sampling period of SAR ADC peripheral, can be used to prevent crosstalk, as it is shown in Figure 5. The gate can be controlled by any pin that has input/output capability. Because the triggering is controlled by a counter, the gate could also be controlled by another timer peripheral output that is configured to be active during the sampling period.

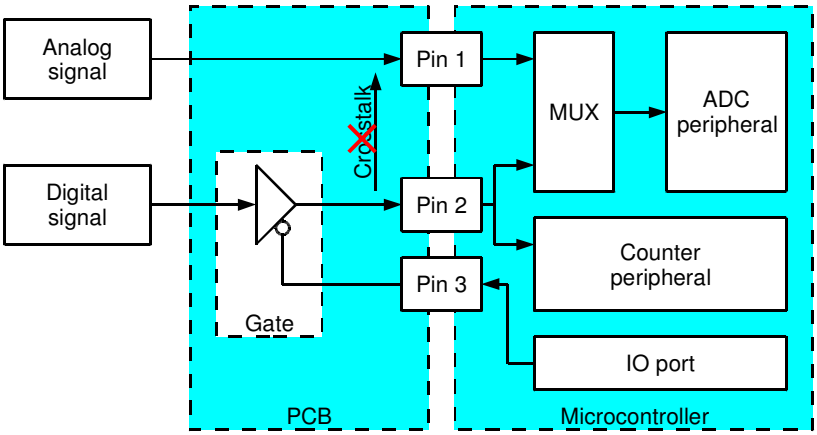

Figure 5. Recommended circuit diagram for asynchronous digital signal connected to a microcontroller.

IV. Conclusions

This paper presents an analog input circuitry and timing of a SAR ADC embedded as a peripheral in a microcontroller. The datasheets of microcontroller very often do not provide sufficient information on ADC.
In a real embedded measurement system, asynchronous digital signals can be present. These signals can be connected to microcontroller and can affect readings of a SAR ADC peripheral conversion. This situation was studied in more details and this interference was measured. From the experimental measurement, a recommended circuit diagram was proposed.
Further work in this field will be focused on other noise sources that can affect SAR ADC results – pin sharing or power supply sharing, for instance. Also some test methods for a SAR ADC peripheral in microcontrollers should be developed because, typically, only a limited and small data memory is available, which excludes usage of standardized test methods [6], [7]. The ADC exponential stimulus histogram test [8] could solve this problem.

References

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