VHDL-AMS Modeling of Continuous-Time Complex Bandpass Delta Sigma Modulator

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Abstract- Continuous-Time delta sigma modulators (CT ΔΣM), by their nature, are mixed-signal systems. That fact creates a discontinuity in the traditional IC design flow which assumes that "discrete" and "continuous" time domain designs require separate design tools. In this work, we present a top level behavioral approach of modeling CT complex Bandpass (CBP) ΔΣM using VHDL-AMS language. The CT ΔΣ model can be used within the analog IC design environment. Fifth-order CT CBP ΔΣM which is tailor made for Bluetooth and WiFi Low-IF receiver demonstrates clearly the modeling technique.

I. Introduction

The development of fully integrated systems for wireless receivers, which consume low power and permit low cost implementations, signifies a major challenge for a lot of analogue designers of the present generation. To better cope with this challenge the low-IF architecture [1] forms the basic topology of many recent receiver architectures. It combines the advantage of a very low IF and a power efficient image rejection without the need for external high Q filtering. Complex sigma-delta A/D converters have an advantage over real signal converters in I/Q (In-phase/Quadrature phase) radio applications in terms of improved stability and large bandwidth. A complex A/D can be designed that has no conjugate poles and zeros, which realize an asymmetric frequency response. The resulting noise transfer function is immune to changes in the center frequency [2]. A lower order complex modulator can then achieve the same performance as higher-order real modulators [2] [3]. Recently, continuous-time ΔΣ ADCs have become very popular because of low power consumption, high speed and small area with respect to their discrete-time counterparts. The fact that CT ΔΣM are mixed-signal systems creates a discontinuity in the traditional IC design flow which assumes that "discrete" and "continuous" time domain designs require separate design tools. In this work, we present a top level behavioral CT ΔΣ model that can be used within the analog IC design environment. Fifth-order CT CBP ΔΣM which is tailor made for Bluetooth and WiFi Low-IF receiver demonstrates clearly the modeling technique.

II. Objectives

More recent developments of the low-IF receiver architecture [1] have concentrated on the digitization of the signal chain with a view to improving multi-mode capability. In an initial realization, this involved positioning the analogue-to-digital converter (ADC) immediately after the mixers of the front end, eliminate the need for automatic gain control (AGC) and move the channel filtering into the digital domain. Hence, to benefit from the obvious merit of this advance, one attractive aspect has proved to be the need for a complex ADC resulting directly from the use of the low IF. The aim of this paper is behavioral modeling of continuous-time quadrature Bandpass ΔΣ modulator for Bluetooth and WiFi standards using low-IF architecture (Figure 1) improved in [4].

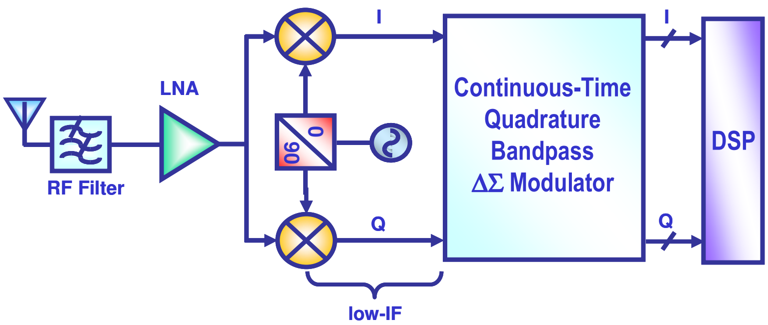
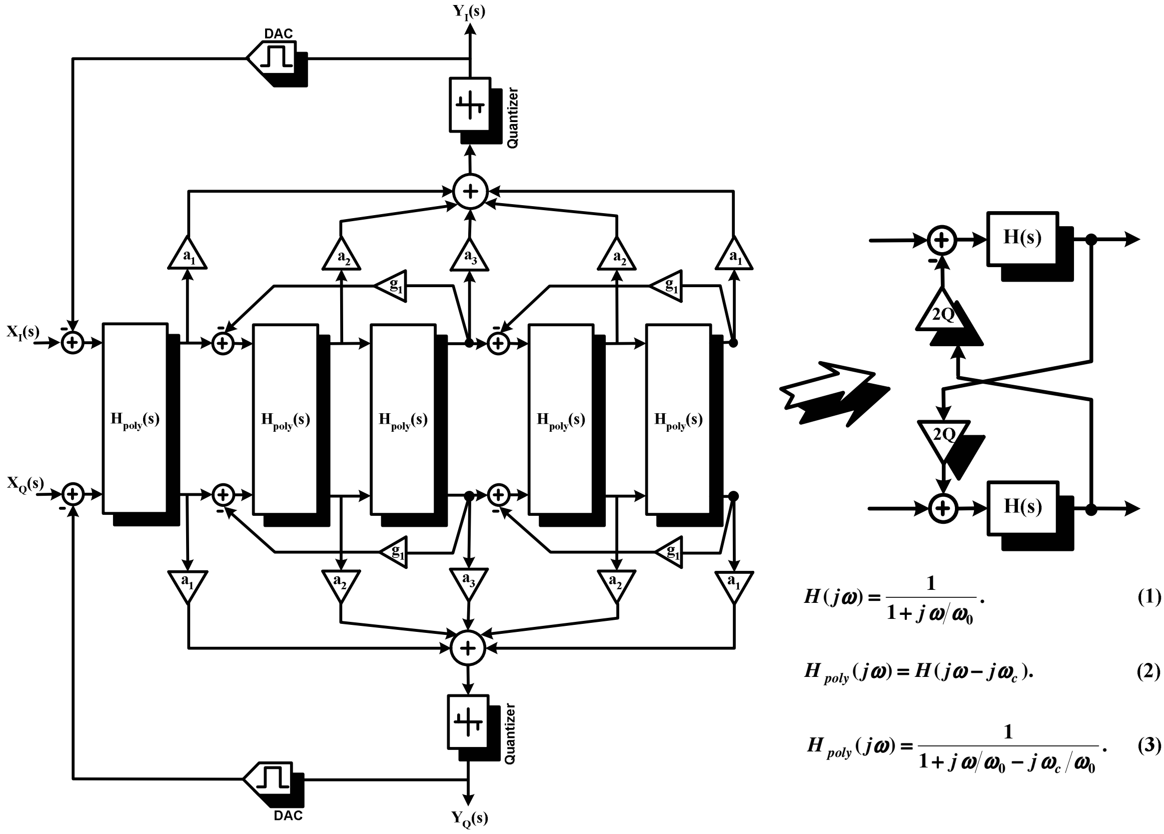


Figure 1. Low-IF receiver architecture operating with one continuous-time quadrature bandpass ΔΣ modulators.

III. Methodology

A. Continuous-Time Complex Bandpass ΔΣ Modulator

A CBP ΔΣM is well suited for use in low-IF receivers [1], [2]. Instead of digitizing the analog $X_I(s)$ and $X_Q(s)$ signals separately with two bandpass modulators, it converts the $X_I(s)$ and $X_Q(s)$ signals at the same time. This is called "complex analog-to-digital (A/D) conversion." Complex-valued signals are not particularly mysterious [1]. They are simply a convenient representation of a pair of real signals. One signal is interpreted as the real part (indicated with subscript or superscript I) and the other signal as the imaginary part (indicated with subscript or superscript Q) of the complex signal. In such a CBP ΔΣM, the same performance is achieved with only half the number of integrators compared to the traditional BP solution [2]. This results in power and area saving. The architecture of CT CBP ΔΣM is shown in Figure 2. It consists of a complex loop filter, two real quantizers, and two real feedback digital-to-analog converters (DACI and DAC_Q). It can be described as a chain of complex integrators with feedforward summation and local resonator feedbacks [4].



$$H(j\omega)=\frac{1}{1+j\,\omega/\omega_0}. \qquad (1)$$

$$H_{poly}(j\omega)=H(j\omega-j\omega_c). \qquad (2)$$

$$H_{poly}(j\omega)=\frac{1}{1+j\,\omega/\omega_0-j\,\omega_c/\omega_0}. \qquad (3)$$

Figure 2. (a) Fifth order CT CPB ΔΣM with feedforward compensation. (b) Block diagram of a complex filter obtained from two cross-coupled lowpass filters.

A complex bandpass filter can be realized by frequency shifting of a lowpass filter. The transfer function of the polyphase filter $H_{poly}(s)$ can be obtained from the lowpass filter H(s) as shown in [1]. The frequency shift in the transfer function is done by cross-coupling of two real filters, which is shown in Figure 2b. Then a single pole complex bandpass filter given in (3) can be derived from the two lowpass filters using (1) and (2). Continuous-time designs studied in this paper are planned using our design strategy proposed in [5]

B. Behavioral Model of CT CBP ΔΣM

The CT CPB ΔΣM is already in itself a mixed-signal system. In this context behavioral simulations are indeed unavoidable. The use of a language like VHDL-AMS which provides a way to use both event-driven and normal circuit simulation is a natural choice [6]. Next, we illustrate some behavioral models of the basic functional blocks required to create a complete CT CBP ΔΣM. Our set of basic blocks consist of the following DT/CT behavioral modules: integrator, general s-transfer function, quantizer, DAC with non-return to zero (NRZ), summing block, ideal gain, and clock. Since the CT CBP ΔΣM is single-bit architecture, it incorporates a clocked quantizer (i.e. comparator) to perform the internal quantization. The VHDL-AMS model of the quantizer is specified [Figure 3a] to exemplify the modeling technique, and to be replaced in a future work by a CMOS circuit in transistor level within 0.35 µm AMS technology. The entity declaration, called quantizer, declares the parameter threshold that defines the comparator level. The threshold is set to 0.0 (Volts) by default. The port interface of the model is mixed: it includes one analog terminal “input” to sense the analog signal to convert and one digital signal “output” to convey the converted value. The architecture body, called single_bit, defines the behavior of the quantizer. The branch quantity vin is declared as the voltage between the analog terminal and the electrical ground. The core of the behavior is a clocked process that is sensitive to the crossing of the level: as soon as the input voltage vin crosses the threshold. The process raises the clock edge, resumes and recomputed the value of the digital output signal output. The notation vin’above(threshold) encodes both the occurrence of an event (when the crossing occurs) and a Boolean value that defines the direction of the crossing (TRUE if the voltage is rising, FALSE if the voltage is falling). When vin’above(threshold) = TRUE the digital output signal is set to the value ’1’, while when vin’above(threshold) = FALSE the digital output signal is set to the value ’0’. The comparator input is driven by a sine wave with a larger period than the clock frequency, again over multiple clock cycles. The conversion process is shown in [Figure 3b].

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-- VHDL-AMS model for Quantizer
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library IEEE;
use IEEE.math_real.all;
library disciplines;
use disciplines.electromagnetic_system.all;

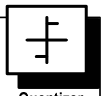
entity quantizer is
      generic (threshod : real := 0.0);
      port (terminal input : electrical;
            signal   clk : in bit;
            signal   output : out bit);
end entity comparator;
-------------------------------------
architecture single_bit of quantizer is

       quantity vin across input to electrical_ground;

begin  -- architeecture single_bit

   clocked: process(clk) is
    begin
       if clk'event and clk ='1' then   -- rising clock edge
         if vin'above(threshod) then
           output <= '1';
         else
           output <= '0';
         end if;
       end if;
    end process clocked;

end architecture single_bit;
```



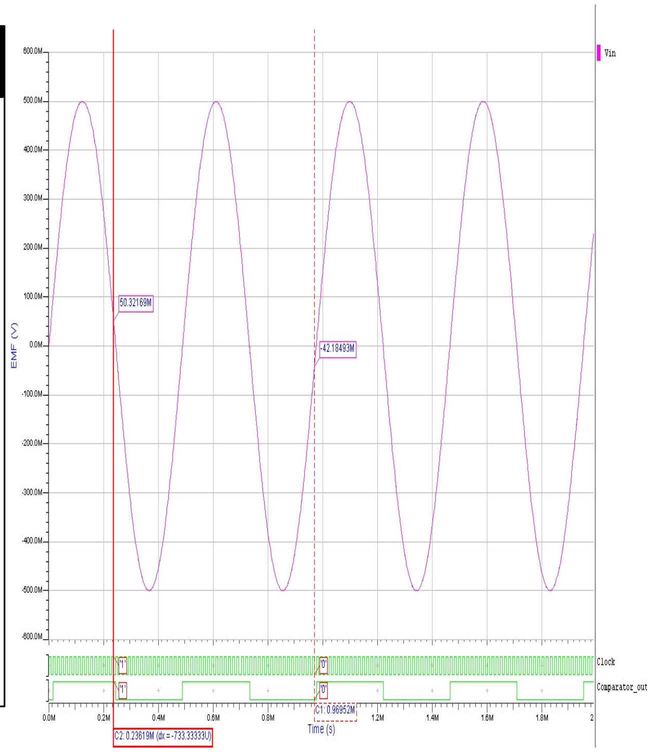


Figure 3. (a) Behavioral model of quantizer. (b) Clocked quantizer when driven by a sine wave.

IV. Simulation Results

We simulated a fifth-order CT CBP ΔΣM, [Figure 2], using the developed behavioral models under design specification in table 1. The I, Q analog input and output bit stream are shown in [Figure 4]. The output spectrum in [Figure 5] shows a complex tone in a noise valley centered at 10 MHz as designed, and fifth notches visible across the band. Note that the spectrum is not symmetrical about DC. The peak SNR achievable for this fifth-order quadrature modulator is 107 dB for Bluetooth and 88 dB for IEEE 802.11b [Figure 6.a]. From linearity viewpoint, the measured IM3 distance for the real modulator is 92 dB [Figure 6.b].

Table 1. Design specifications

Sampling Frequency	160 MHz	
Center Frequency	10 MHz	
Standard	Bluetooth	WiFi
Signal Bandwidth	0.5 MHz	10 MHz
Oversampling Ratio (OSR)	160	8

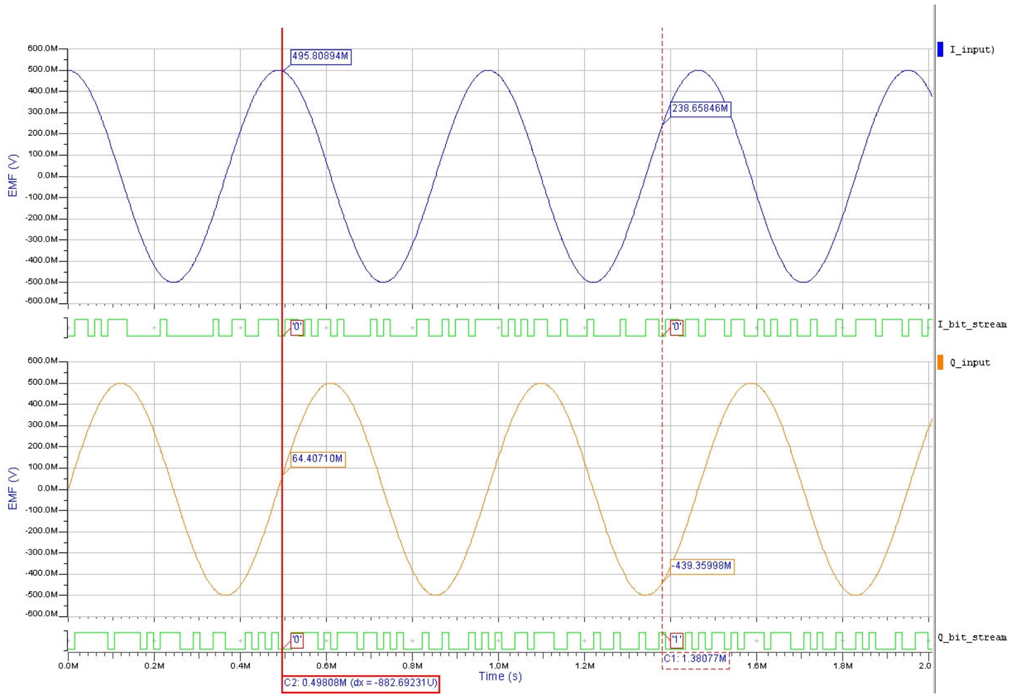


Figure 4. I, Q analog input and I, Q output bit stream.

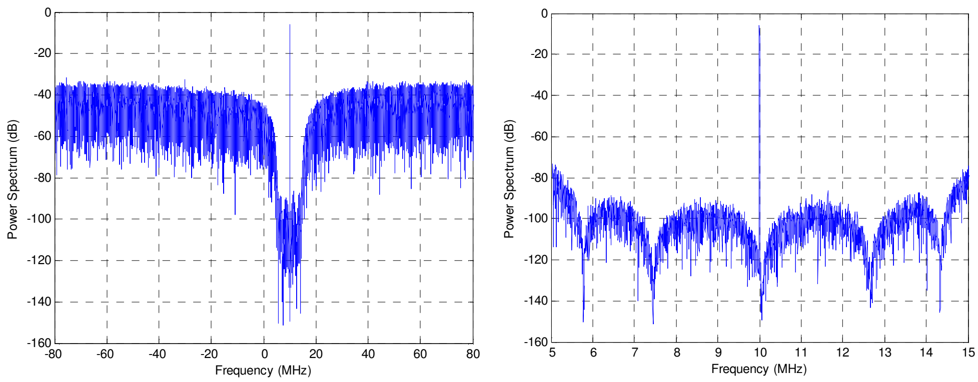


Figure 5. Output spectrum of the CT CBP ΔΣM, close-up view of the in band.

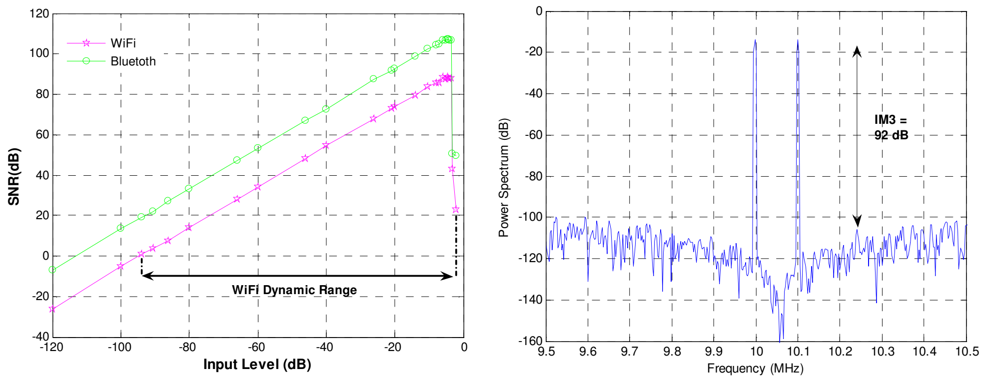


Figure 6. (a) SNR performance, and (b) measured intermodulation distortion with -6 dBFS input signals for fifth-order CT CBP ΔΣM.

V. Conclusions

A top level behavioral approach of modeling of CT CBP ΔΣM using VHDL-AMS language is presented. A mixed-signal behavioral model for a fifth-order CT CBP ΔΣM circuit has been presented with aim in the quantizer model which possibly can be replaced by a CMOS circuit in transistor level. It has been shown that by using mixed-signal approach for behavioral modeling one can achieve high simulation speed and produce meaningful results by staying within one design environment throughout the design process. The quadrature modulator achieves good performance and can be integrated in the low-IF architecture for Bluetooth and WiFi receiver.

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