Reference Folding Subranging Caliper ADC

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Abstract- The paper presents a reduced ADC architecture obtained by introducing the subranging technique into the scheme of a caliper AD converter. This last converter was already proposed as an application of a theory which describes the comparison between scales having the steps prime each other. This converter architecture drastically reduces the number of the required resistors for a full flash realization. The introduction of the subranging technique into the caliper ADC here presented reduces also the number of the required comparators. The result is a very compact architecture. The paper describes a first intention architecture based on ideal components. An example of SPICE simulation is given.

I. Introduction

Some computer evaluations of time behavior of physical quantities require a great speed in analog to digital conversion and suggest the use of a full flash ADC. The realization of this kind of converter requires a great number of comparators and resistors, namely 2^n if n is the number of bits of the requested wordlength. Obviously, if a great wordlength is requested, a lot of practical and technological problems occur and a trade off between the conversion speed and the circuitry size should be found.
Some years ago the subranging technique was proposed. This technique allows the reduction of the number of the required comparators in a full flash architecture, i.e. an architecture which realizes the conversion in a single clock period. However, the maximum of the possible clock speed is reduced. An example of subranging full flash realization was given in [1]. However, this architecture requires a great number of switches.
Recently the caliper converter architecture was presented as a way to drastically reduce the number of resistors in a full flash converter realization [2-4]. This reduction is obtained without significant reduction of the speed properties of the whole architecture.
This paper describes a converter architecture obtained by introducing the subranging technique in the caliper architecture. As a result, a very compact and interesting architecture has been obtained. The speed properties of this composed architecture are similar to the subranging ones. Further, by suffering an amount of the single sample conversion time, i.e. a reduction of the maximum allowed clock speed, the number of the requested switches can be greatly reduced.
Section 2, recalling the full flash "classical" architecture for the sake of clarity, simply describes the two above mentioned ones to be mixed. The resulting architecture is described in section 3. Section 4 shows the main properties of the proposed architecture.

II. Classical, subranging and caliper architectures

To clearly compare the three architectures, classical, subranging, and caliper respectively, we refer to figure 1: it shows three example of the cited architectures for a supposed binary conversion of four bits. In figure 1-a) a classical full flash ADC architecture is reported: a series of sixteen resistors driven by a suitable voltage reference sources provides sixteen voltage reference levels. A set of fifteen comparators realizes a thermometric scale. The input level to be converted is compared by the reference voltage levels using the set of comparators. The number of "on" comparators is then converted into a binary word (fifteen comparators = four bits) using a logical network, here not reported. In figure 1-b) the architecture of the caliper converter is shown: the fifteen comparators are set by the coincidences of the two scales, the fix and the mobile, which is driven by the input signal applied to two OP-AMP. Also in this case, the number of "on" comparators is converted into a binary word by a logical network, not reported in the picture. Figure 1-c) shows the subranging architecture:

the thermometric scale formed by the comparators is splitted in two parts: the first one determines the most significant bits and the second determines the remaining two bits. A simple analogue logic drives the sets of switches which realize a folding on the reference voltage so that the second set of comparators operates starting from the already converted voltage. The whole conversion is completed in a clock period but the maximum permitted clock soeed results greatly reduced. However, also the number of the requested comparators is greatly reduced.

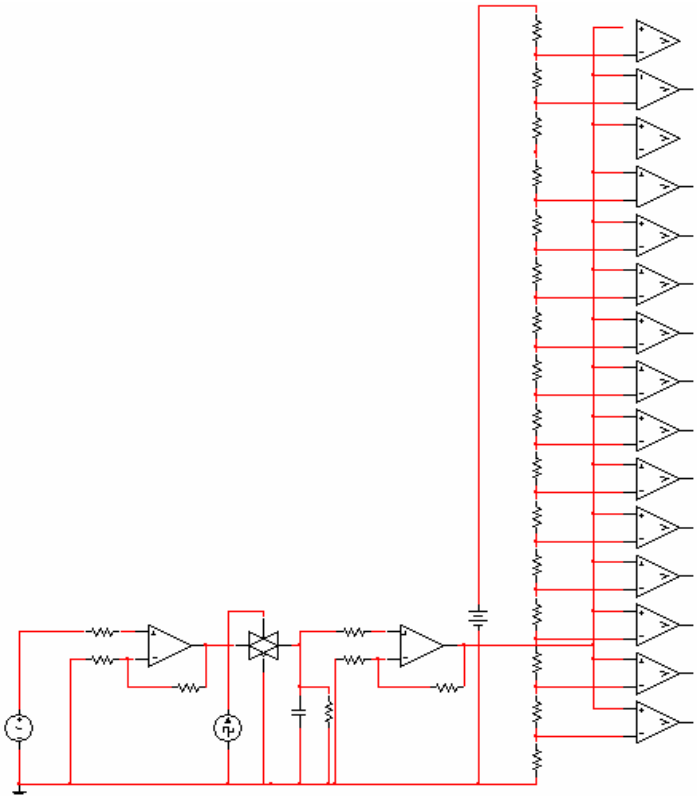

Figure 1-a) classical architecture of the full flash converter.

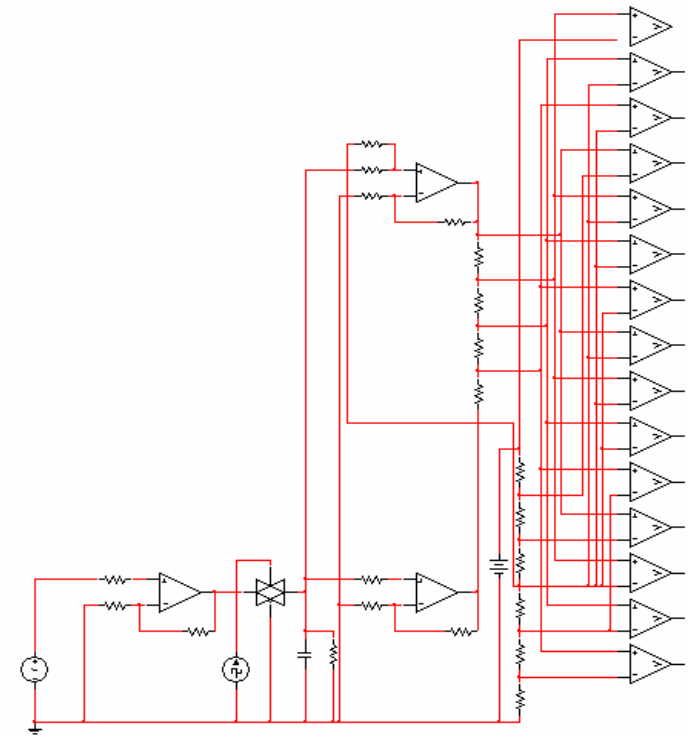

Figure 1-b) – caliper converter;

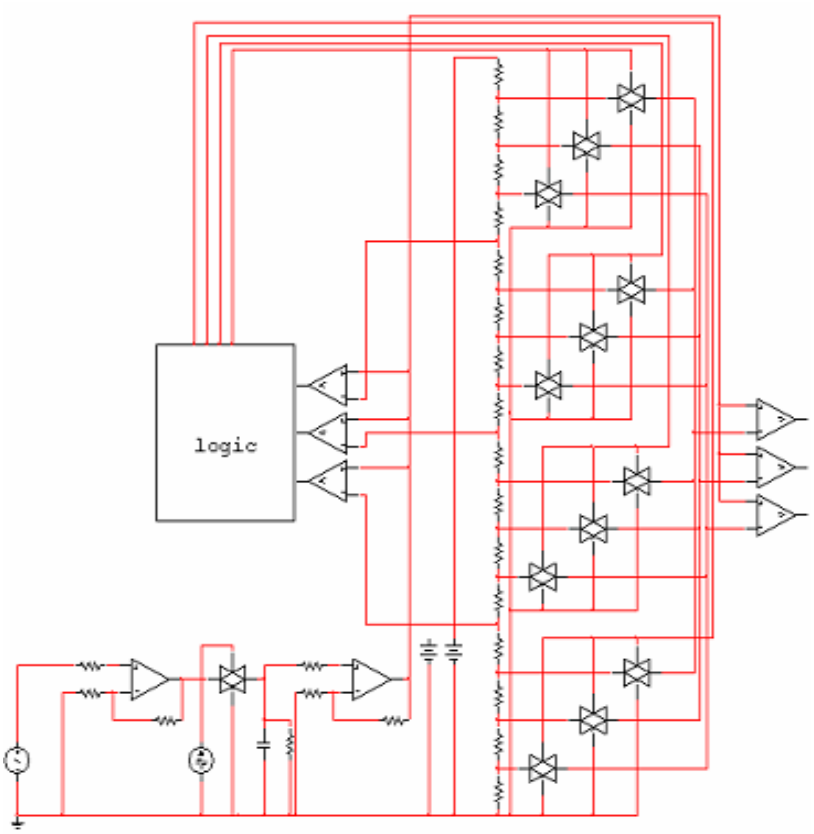

Figure 1-c) – subranging architecture. All the converters realize a thermometric scale (two reduced thermometric scales in the case of the subranging architecture (c)).

III. Proposed architecture

The proposed architecture attempts to obtain the favorable features of both the starting architectures, i.e. the drastic reduction of the number of the required resistors, as in the caliper architecture, and the drastic reduction of the number of the required comparators, as in the subranging architecture. Further, a particular feature of the proposed architecture is the reduction of the number of the switches with respect to the subranging architecture. A simple scheme of the proposed architecture is given in figure 2. This scheme regards a four bit converter as the analogue of figure 1.

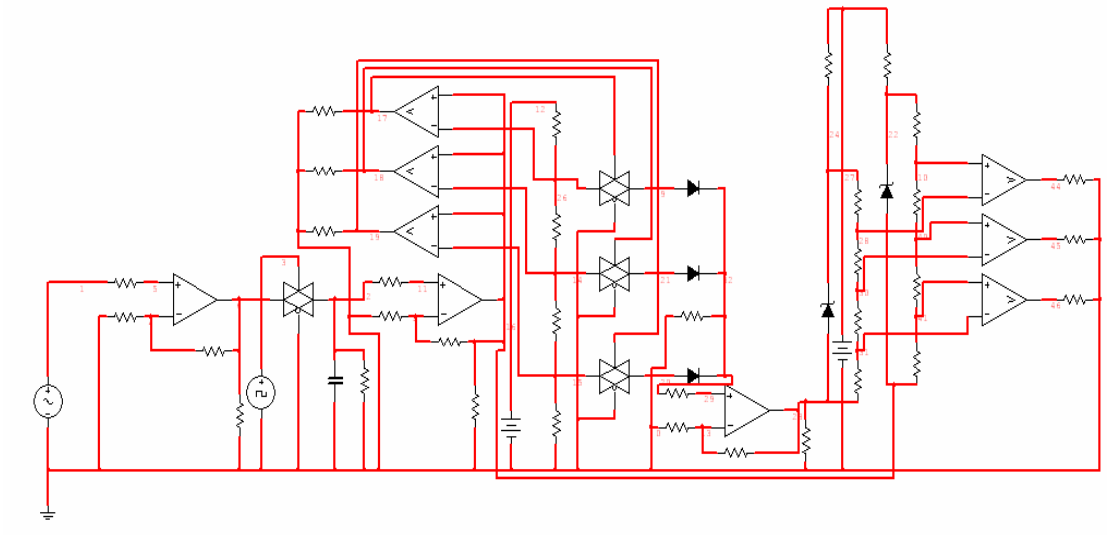

Figure 2-Proposed architecture.

IV. Main properties of the proposed architecture

The philosophy followed in the conversion can be described with reference to figure 2. On the far left we have an AC source which represents the signal to be converted. A classical scheme of the sample-hold (SH) circuit is used and the second OP-AMP of this SH directly drives a mobile scale (on the far right) which is used for the determination of the least significant bits (LSB). The sampled signal emerging from the SH is compared with the voltage levels of a fixed scale (in the middle of the scheme) driven by a reference source: three comparators form a thermometric scale to be converted in binary to obtain the two main bits. These comparators also drive a set of switches which generates three voltage levels. These voltages are used to drive a three positions “fix scale” which realizes the “folding” of the reference levels. The mobile one is then compared with this scale and the obtained coincidences are detected by the thermometric scale of comparators in the far right. This last has to be converterd in binary to give the LSBs. As clearly it appears in the scheme, also the number of required switches is greatly reduced.
The validity of the proposed conversion philosophy, which is the basis of the simple architecture of figure 2, has been proved by SPICE simulations. An example of these simulations is given in figure 3.

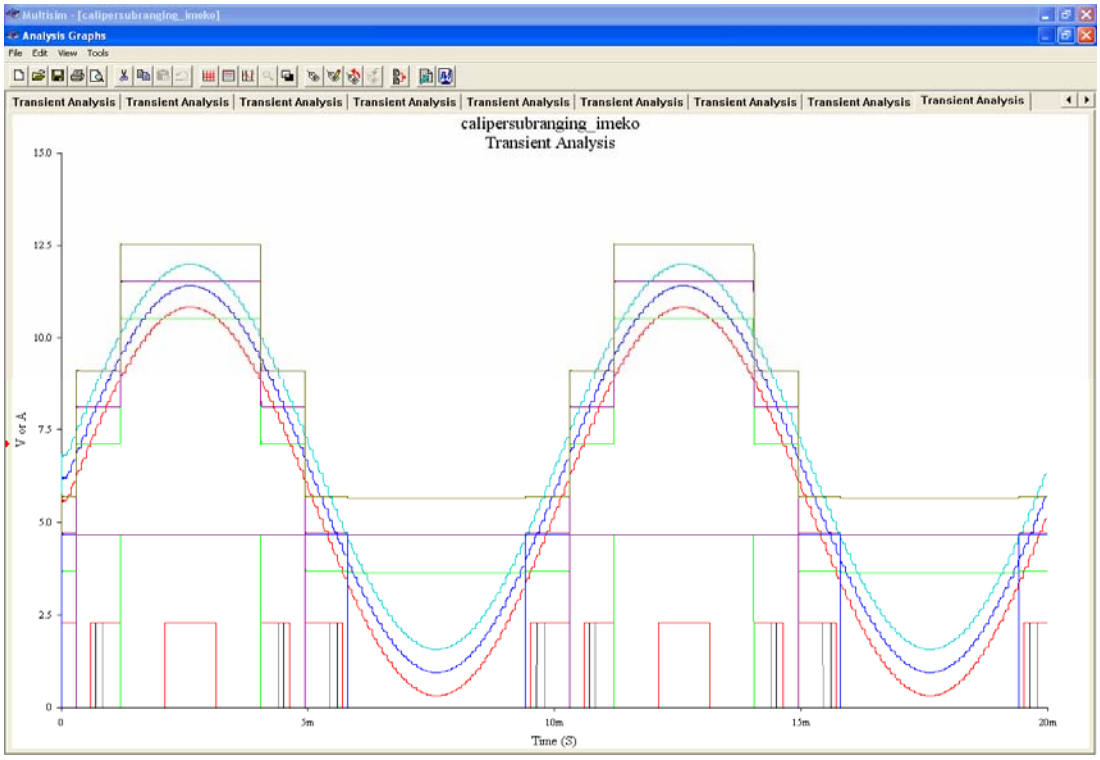

Figure 3-Transient behavior of the proposed architecture example: the sinusoidal lines represent the input sinusoidal signal splitted in three levels by the mobile scale; the upper horizontal segments represent the voltage levels of the three positions fix scale; the rectangles in the low part of the figure represent the behavior of the comparators: these on the left scale (MSB) are driven by a major voltage, with respect to those in the right scale (LSB), and determine the “folding” of the reference scale.

V. Remarks and conclusions

The proposed architecture presents, in terms of the circuit complexity, the combined advantages of both the starting architectures, namely caliper architecture and subranging architecure. The first one allows the reduction of the number of required resistors which realize the scale of reference voltage levels. The second one reduces the number of the required comparators. A further improvement can be obtained if the “folding” of the input signal, that is a required characteristic of the subranging architecture, is transferred to the reference scale of voltage levels. The given example realizes this transfer and shows that this technique can reduce the number of the required switches. However, the circuitry given in the example is simply demonstrative of the proposed conversion philosophy. An useful realization requires a solid development.

References

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