VHDL-AMS Behavioral Modeling of High-Speed Continuous-Time Delta-Sigma Modulator

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Abstract- An advanced design methodology using a combination of behavioral models and transistor level models is presented in this paper. This methodology is very interesting for complex mixed-signal IC design, reducing the simulation time and improving the design flexibility. In order to validate the methodology proposed, a High-Speed Bandpass Continuous-Time Delta-Sigma Modulator is modeled. This modulator samples at high-IF signals, performing the direct conversion in the modern RF front-end receivers.

I. Introduction

The emergent demand for personal communication devices and services has led to the emergence of several wireless standards. In order to accommodate these different wireless standards, multi-standard mobile terminals are highly demanded. RF front-end receiver architectures tend to get closer the Analog-to-Digital (A/D) interface as near as possible to the antenna. This evolution allows a direct conversion of an analog signal into digital at high intermediate frequencies (IF), simplifying the overall system design and alleviating the issues linked with IF mixers. Bandpass Delta-Sigma modulators sampling at high-IF allow reducing analog hardware and further realization of fully-integrated software-programmable RF receivers (SDR – Software Defined Radio). For this reason, several published single-bit Continuous-Time Delta-Sigma modulators can digitize signals from 800MHz to 1GHz [1-3].
The convergence of computer and communication products had led to a mixed-signal ICs continuously growing in complexity. The time-to-market becomes very short and efficient design methodologies are required. Despite the fact that many electronic systems are fully-digital, there are many that incorporate an analog part to interface to the "real world". The growth interaction of analog and digital devices calls for the use of top-down design methodologies, resulting in behavioral modeling at different levels of abstraction. The simulation of a complex system with digital and analog parts is not practical on the transistor level. The possibility of merging behavioral modeling blocks and transistor level blocks can optimize the simulation speed and reduce the design time.
For the first time, a new mixed-signal HDL standard VHDL-AMS was approved in March 1999. This standard allows the utilization of VHDL-AMS to build complex analog and mixed-signal models by combining differential equations, algebraic constraints and logical controls [4].
A VHDL-AMS behavioral model of a High-Speed Multi-bit Continuous-Time Delta-Sigma Modulator is presented in this paper. An advanced design methodology using a combination of top-down and bottom-up approaches is used in order to optimize the simulation time and to improve the design flexibility.

II. Continuous-Time Delta-Sigma Modulator Architecture

The architecture proposed is based on an association of resonators [$H(s) = As/(s^2+\omega_o^2)$] with two different types of feedback Digital-to-Analog Converter (DAC). It offers a full control over the noise-shaping behavior, leading to the so-called *multi-feedback architecture*. This architecture allows the achievement of a higher order noise-shaping which maintains the modulator stability. The DAC used are return-to-zero (RZ) and half-return-to-zero (HRZ). The quantizer implements a 3-bit flash architecture. We choose a 3-bit quantizer instead of a usual 1-bit quantizer in order to reduce the quantization noise and to improve stability, at the cost of introducing mismatch errors [5]. The quantizer employs an input adapter amplifier, seven comparators (one per comparison level) with associated latches, an encoder matrix and three output buffers. Figure 1 shows the Continuous-Time Delta-Sigma modulator architecture.

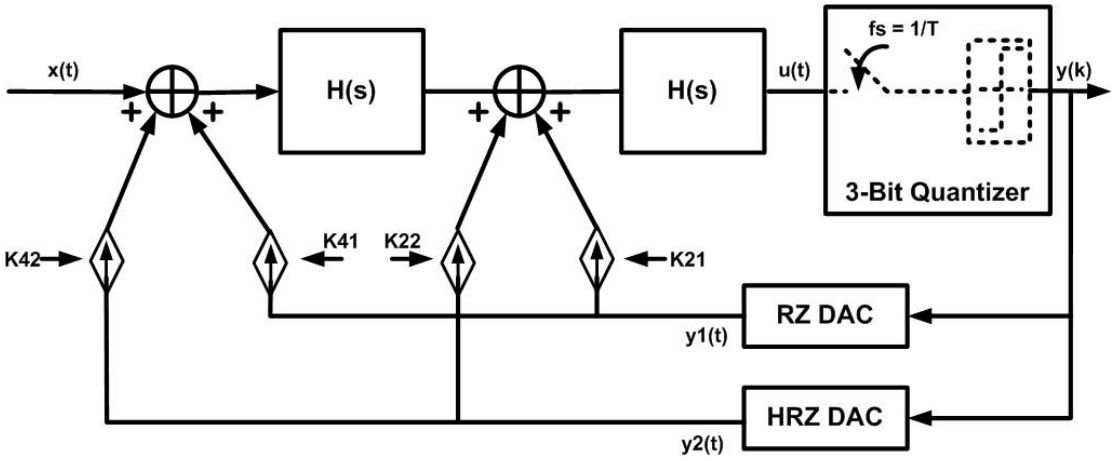

Figure 1. Continuous-Time Delta-Sigma Modulator Architecture

III. Modeling and Simulation Methodology

One of the main problems of the ΔΣ modulator is the difficulty to predict the converter resolution by analytical means, thus relying on transient simulations for obtaining its performance [6]. However, the large oversampling ratio used in the modulators and the requested accuracy demands a lot of time with SPICE-like simulators to perform the transient simulation, which makes it unfeasible. To avoid these problems, an advanced design methodology is used.

The process starts from the Continuous-Time Delta-Sigma modulator system specification and simulation at the top-level abstraction. Then, a top-down approach is applied, replacing certain ideal blocks with non-ideal models or even their SPICE representation to obtain greater accuracy. Each building-block of the Continuous-Time Delta-Sigma modulator (Figure 1) is modeled using a VHDL-AMS language. The VHDL-AMS codes are compiled using the ADVance MS compilator. The resulting behavioral models are converted in functional VHDL-AMS blocks to be used in the CADENCE environment. This design methodology allows the mixing of behavioral models and transistor level models in the same simulation environment (CADENCE), improving the simulation speed. The modulator output is obtained both in the time domain and in the frequency domain (through FFT). These simulations run with ADVance MS (ADMS) under CADENCE environment. Figure 2 shows the design methodology using both ADVance MS and CADENCE.

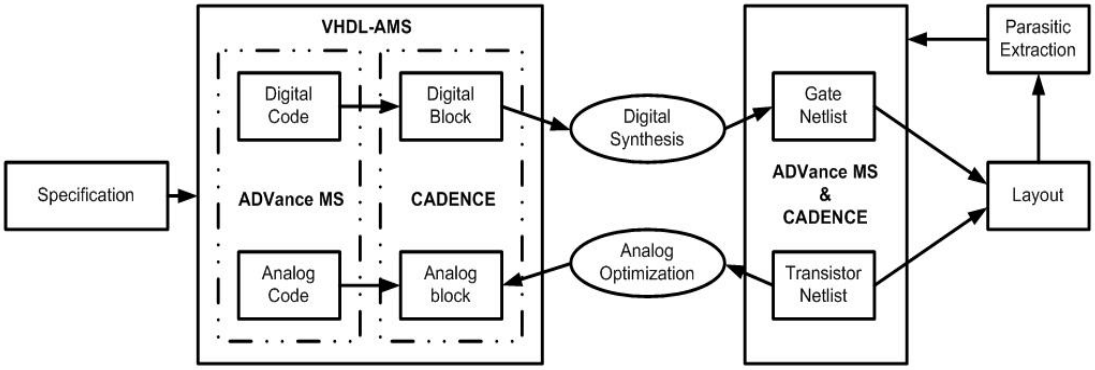

Figure 2. Design Methodology mixing behavioral models with transistor level models

IV. Simulation Results

The overall modulator was simulated using ADVANCE MS simulator under CADENCE. Figure 3 shows an example of simulation using transistor level blocks (sampling stage) and behavioral models (comparators). The comparators transform the input analog signal into continuous-time digital data, before facing the sampling stage. Comparison is in effect a binary phenomenon that produces a logic output of ONE or ZERO depending on the polarity of a given input. This characteristic is modeled based on an infinite gain amplifier. The sampling stage utilizes an association of D-latches, which

memorizes the state of the comparators at a given instant defined by the clock. In Figure 3, after each comparator (VHDL-AMS model), two D-latches (transistor level) in a master-slave configuration (DFF) perform the sampling function. The combination of transistor level and VHDL-AMS models reduces the simulation time and improve the design flexibility.
Feedback coefficients were determined by matching a Continuous-Time impulse response of a SIMULINK model to an equivalent Discrete-Time modulator [7]. Table 1 presents the parameters used in the simulations.

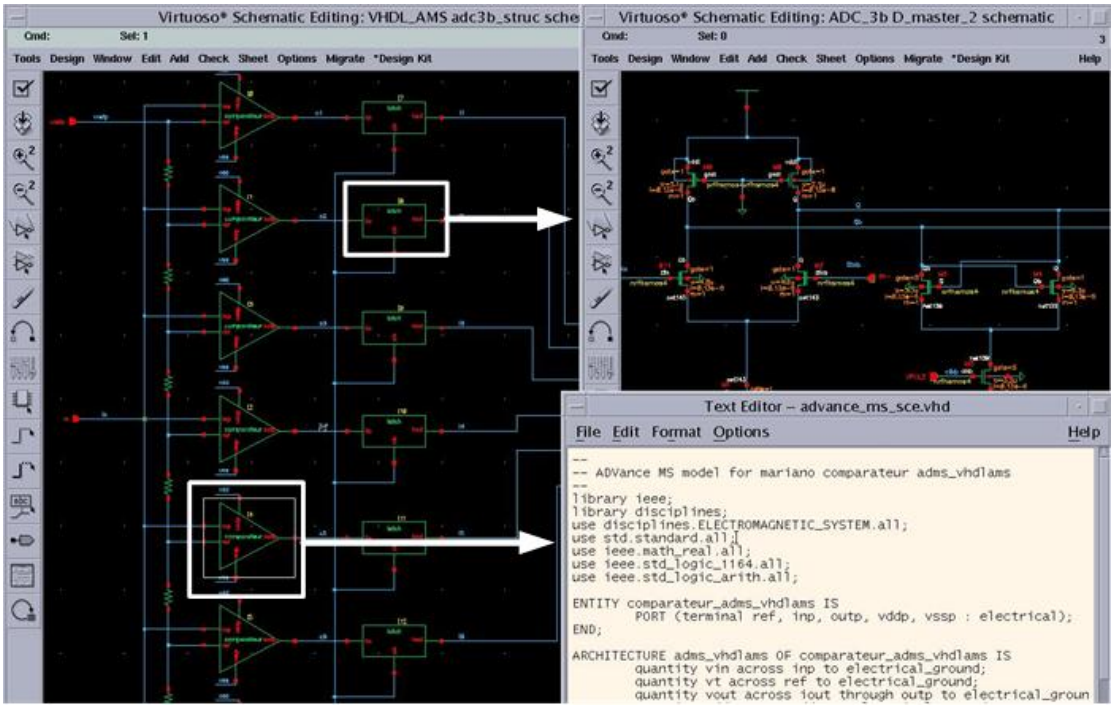

Figure 3. Overall system simulation using transistor level and VHDL-AMS models

Parameters	**Value**
Input Signal	1 GHz
Modulator Bandwidth	20 MHz
Sampling Frequency	4 GHz
Modulator Resolution	3 bits
OSR	100

Table 1. Simulation Parameters

The Continuous-Time Delta-Sigma modulator is able to directly digitize a 1GHz input signal in a 20MHz bandwidth, with dynamic range (DR) of 87dB. The SNR in a 1 MHz bandwidth extrapolates 100 dB. Figure 4 shows the simulated output spectrum of the ΔΣ modulator.

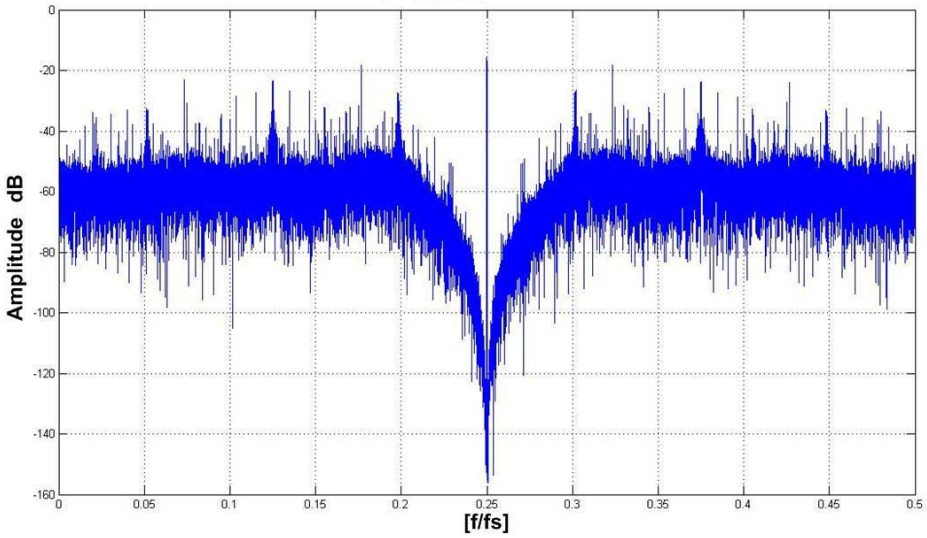

Figure 4. Output Spectrum of the CT Bandpass Delta-Sigma Modulator

V. Conclusion

A VHDL-AMS behavioral model of a High-Speed Multi-bit Continuous-Time Delta-Sigma Modulator is presented in this paper. An advanced design methodology using a combination of behavioral models and transistor level models is used in order to reduce the simulation time and to improve the design flexibility. The Continuous-Time Delta-Sigma modulator is able to directly digitize a 1GHz input signal in a 20MHz bandwidth, with dynamic range of 87dB.

References

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