2.5 V, 10-bit, 50-MS/s CMOS Pipeline Low Power A/D Converter

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Abstract

In this paper, we present A/D converter for signal processing of infrared sensor and CMOS image sensor. The A/D converter implemented in a 0.25um CMOS process provides a resolution of 10bits at a sampling rate of 50MS/s while dissipating 67mW from 2.5V supply voltage.
This A/D converter is based on a pipelined architecture in which the number of bits converted per stage and the stage number are optimized to simultaneously achieve the desired linearity and reduce power consumption as well. Simulation results show that the A/D converter using 1.5bit per stage MDAC with switched capacitors and dynamic comparators efficiently reduces the power consumption.

***Keywords*:** Analog-to-digital converter, pipeline ADC, MDAC, switched-capacitor circuits, 1.5bit per stage.

1. Introduction

As the use of DSP based devices grows rapidly, the need to implement A/D interfaces beside digital CMOS core becomes more significant. Low power A/D converter with high-speed operation and smaller area is required as process feature is scaling down to contain many image pixels in one chip image sensor and pixel number is increasing to obtain more wide image. Pipeline architecture is chosen due to its balance between power and performance. In pipeline converters, power consumption can be optimized by an appropriate selection of bits/stage [1]-[3]. Employing switched-capacitor (SC) technique, it is well compatible with digital CMOS process. General pipelined architecture consists of N stages in which M bits are resolved in each stage and usually one bit of M bits is overlapped in next stages, which relaxes the comparator's offset condition. Since 1.5bit per stage-pipelined structure gives power-optimized per stage resolution and relaxes the requirement for the sub-AD comparator, sub-DAC, and residual gain amplifier [5-6], we use it in this paper.

In the following sections, we describe the architecture of designed A/D converter and discuss several techniques of circuit design. Simulation results of using HSPICE and MATLAB show the efficiency of the designed converter.

2. ADC Architecture

Architecture of a designed A/D converter is shown in Fig.1. This A/D converter consists of seven 1.5-bit stages and finally the pipeline is terminated with a 3bits flash, one MSB of error correction bit and two effective data bit. In Fig.1, each stage from stage-1 to stage-7 of input sample-hold block and sub-DAC, residual gain amp are integrated to MDAC block, which is the key circuit in the pipeline A/D converter. In 1.5bit per stage architecture, two bits are resolved in each stage. Sub-DAC subtracts the DAC output from the sampled input and amplifies the resulting residue by a gain of two. It is very important that closed loop gain has to maintain exactly two in order to maintain system linearity and resolution. Gain error comes from the finite op-amp gain, input parasitic capacitor and the capacitor mismatch. The input signal ranges from –Vref to +Vref and the sub-ADC decision points are chosen at +1/4Vref and -1/4Vref. Depending on sub-ADC decision, one of three DAC level (+Vref, 0, -Vref) is chosen. An over-range value of Vref/2 is obtained, and comparator offset error of Vref/4 can be tolerated. The input-output transfer function for a 1.5bit per stage is as shown in Fig.2. The output bits of each stage are delayed properly in a shift register of Delay Element block and fed into an adder that performs the error correction algorithm described in [7].

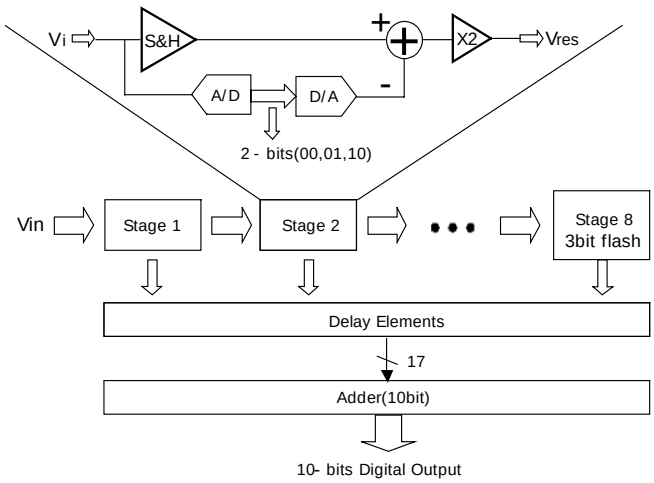

Fig. 1. Block diagram of a designed A/D converter.

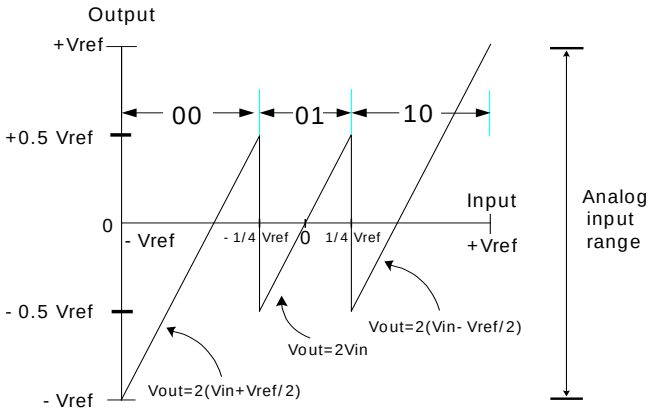

Fig. 2. Input-output transfer function for 1.5bit per stage

3. Circuit Design

A. Op-amp design

A modest open loop DC gain as well as a high gain bandwidth (GBW) is needed for a 10bits resolution and high-speed pipeline A/D converter. The best architecture for a high-speed op-amp is the telescopic cascode. It consumes lower power than any other architecture as well as having a good phase margin. However, it requires a large supply voltage caused by the transistor stacking. By the restriction of low supply voltages, therefore, a telescopic amp with sufficient gain is severely limited in signal swing. Therefore, to maximize dynamic output range with low supply voltage and low power consumption, we designed folded cascode amplifier. Denoting the error caused by the finite open loop DC gain of op-amp (Ao) in each stage of a 1.5bit/stage pipeline A/D converter as ε, the total error of the converter reduced in the input is also equal to ε. To assure a total error is less than 1LSB in the input of the converter, the open loop DC gain of the op-amp is designed nominally to 65dB giving some margin for the process variations. The output of each stage must settle to 10-bit accuracy within a half of a clock cycle. Taking the limited slew-rate into account, the amplifiers are designed to have GBW of 300MHz. Designed folded cascode amp is illustrated in Fig.3 and the simulation results of it are shown in Fig.4.

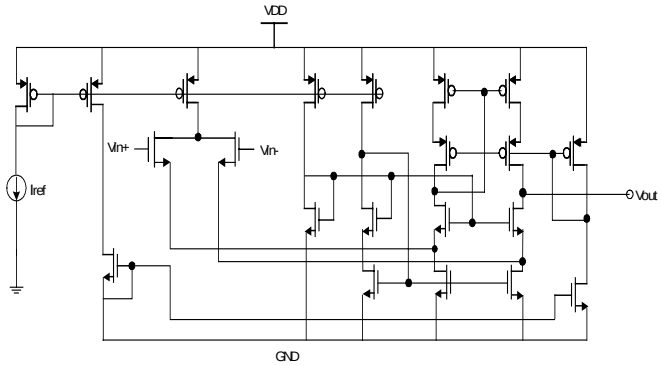

Fig. 3. Folded cascode op-amp

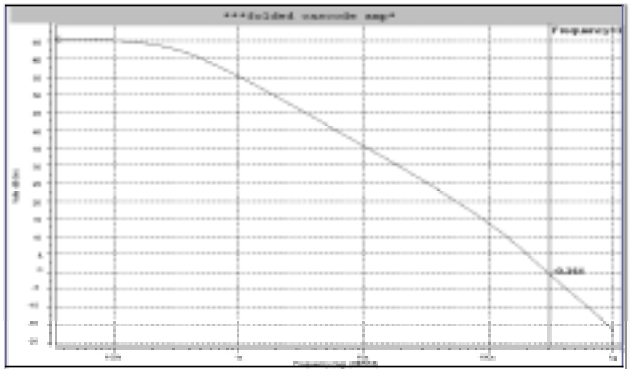

Fig. 4. Simulated performance result.

B. 1.5bit pipeline stage design

As mentioned above, each stage of 1.5bit pipeline A/D converter is consisted of the multiplying digital-to-analog converter (MDAC) and sub-ADC. The 1.5bit pipeline stage circuit and its clock phase are described in Fig. 5 and Fig. 6, respectively. MDAC includes input sample-hold block, sub-DAC, and residual gain amp that is implemented by switched-capacitor amplifier and uses two identical capacitors for sampling and amplifying for an accurate stage gain (closed loop) of two. In order to subtract sub-DAC level from the sampled input, Mux_out is controlled by sub-ADC value. During the sampling phase (clk1), Cs and Cf sample the analog signal Vin from the previous stage and the amplifier is auto-zeroed by connecting it in a unity-gain feedback configuration in order to reduce input offset. During the amplifying phase (clk2), the feedback capacitor Cf is connected around the amplifier whereas the bottom plate of Cs is connected to Mux_out (+Vref, Vcm, -Vref) depending in the sub-ADC output level. The accuracy of the interstage sampling, subtracting, and gain circuit operation depends on the matching between the interstage capacitors Cs, Cf, and the performance of the op-amp circuit.

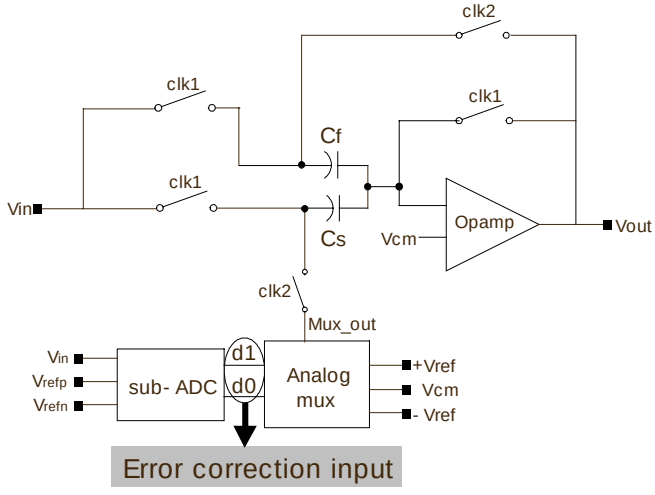

Fig. 5. 1.5bit pipeline stage circuit

To maximize the matching between the two capacitors and to minimize bottom plate parasitic, the capacitors are realized using a centroid layout and stacks of metal layers without using poly-silicon or diffused layer. The feedback factor in MDAC circuit that is operated in the closed loop configuration is nearly the value of 0.4. The Sub-ADC is consisted of two comparators and thermometer encoder that converts thermo-code (00,01,11) to binary-code (00,01,10). The threshold voltages of the two comparators are –Vref/4 and +Vref/4, respectively. In order to reduce the effect of output delay of sub-ADC, latch clock of comparator is clk1p that is turned off slightly before clk1.

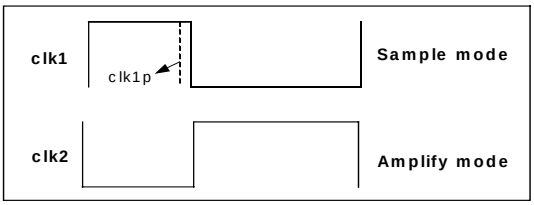

Fig. 6. Clock phase of 1.5 bit pipeline stage

C. Comparator Design

Fig. 7 shows the comparator circuit, which is consisted of a preamplifier followed by a dynamic latched circuit and buffer [8], and is used in the sub-ADC. Using such architecture improves metastability and reduces kick-back noise on the input signal. The resolution of designed comparator is 0.5mV and output reaches the logic levels in 2ns delay. When clk1p signal is high, input tracking and output reset (GND) are carried out while latch and decision are carried out when clk1p signal is low. If small signal trans-conductance of MP1, MP2 is g_{m1}, g_{m2} respectively in Fig. 7, voltage gain of preamp Av is given by

$$A_v = \frac{g_{m1}}{g_{m2}} = \sqrt{\frac{u_n(W/L)_1}{u_p(W/L)_2}}$$

Considering 10bits resolution and taking 50MS/s conversion speed, preamp gain is chosen to 15.8dB. Even though the increment of preamp gain causes the increment of resolution of comparator, latching speed can be limited since the increment of time-constant looking into preamp output node is relatively higher than that of resolution of comparator.

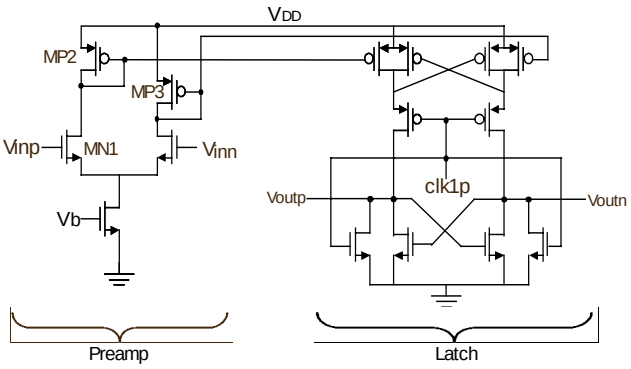

Fig. 7. Designed comparator circuit.

4. Full chip simulation results

The dynamic range of input signal is chosen to be 1Vpp. Fig. 8 shows 5MHz sine wave full scale input and its reconstructed output by the ideal D/A converter. In the figure, we see that the designed A/D converter has 50MS/s conversion speed and 5-clock period latency. In addition, the integral nonlinearity (INL) and differential nonlinearity (DNL) are found to be 1.3 LSB and 0.7 LSB, respectively.

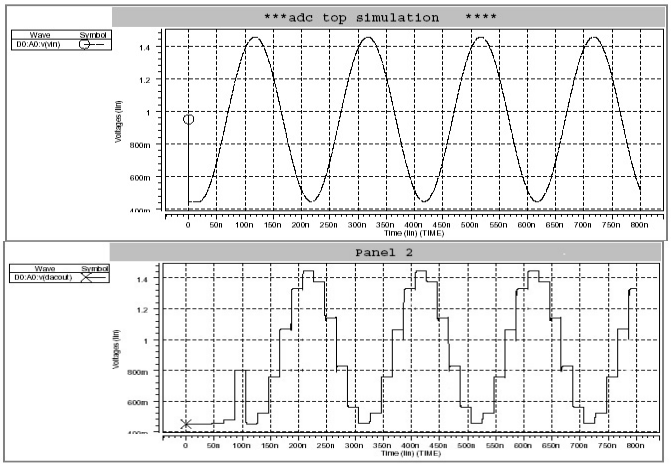

Fig. 8. Sine wave (5MHz) and its output at 50MS/s.

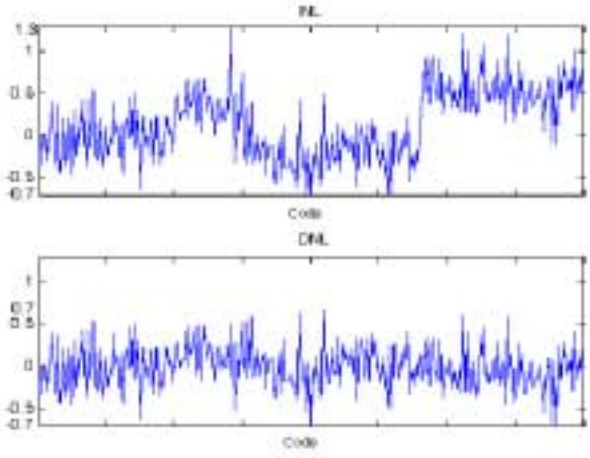

Fig. 9. Static characteristics at 50MS/s.

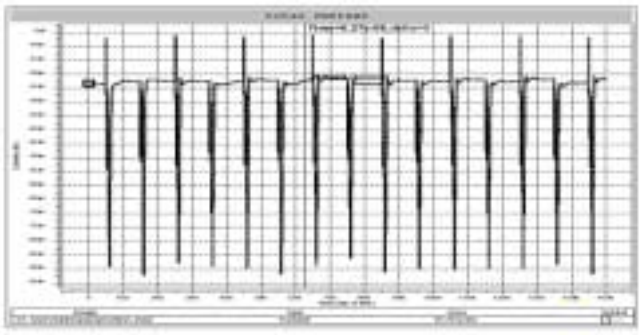

Fig. 10. Total current consumption.

The forms of the INL and DNL curves are shown in Fig.9. The measured total current consumption in Fig.9 is 26.8mA from 2.5V supply giving a power dissipation of 67mW.

5. Conclusion

Table. 1. Specification of the A/D converter

Specification	This work
Process technology	0.25um CMOS
Architecture	1.5bit per stage pipeline
Resolution	10 bit
Supply voltage	2.5V
Sampling speed	50MS/s
Full scale input range	1Vpp
Power dissipation	67mW
INL	1.3LSB
DNL	0.7LSB

In this paper, we described the design and implementation of a 10-bits, 50-MS/s pipeline ADC in 0.25um CMOS process. Table.1 summarizes spec of the A/D converter. By combining all 8 stages in pipeline, we get a 10bits analog-digital conversion. To minimize the power while maintaining the desired speed, the 1.5bit per stage architecture is selected and finally the pipeline is terminated with a 3bits flash. The prototype is on fabrication in 0.25um CMOS technology.

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