A 14-BIT BANDPASS MASH SIGMA-DELTA PIPELINE A/D CONVERTER

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ABSTRACT

In this paper a two stage bandpass MASH (multi-stage noise shaping) sigma-delta (ΣΔ) modulator is presented. A resolution of 14 bits has been achieved over a 5 MHz band around an intermediate frequency (IF) of 20 MHz with a clock frequency of 80 MHz. This performance is obtained using a 6-th order bandpass ΣΔ modulator followed by a 10 bit pipeline converter. The proposed circuit has been extensively simulated, both at behavioral and at circuit level, and results are illustrated.

1. INTRODUCTION

Direct analog-to-digital (A/D) conversion of band-limited signals centered at intermediate frequency (IF) by oversampling converters is becoming very popular in telecommunication systems, especially in wide-band base transceiver station (BTS) receivers based on the software radio (SWR) technique [1]. These A/D converters (ADCs) have to achieve challenging specifications, particularly in terms of signal-to-noise ratio (*SNR*), sampling jitter and spurious-free dynamic range (*SFDR*). The most important specifications of such an A/D converter are summarized in Tab. 1.

Multi-bit bandpass sigma-delta (ΣΔ) modulators are typically used for these applications, since they allow us to digitize only the band of interest around IF. However, the large signal bandwidth typical of third generation mobile communication systems limits the available oversampling ratio to fairly low values. Therefore, in order to achieve the required resolution, we have to use either high-order modulators or a large number of bits in the quantizer. Both of these solutions impose severe constraints either on stability or linearity, thus making the design quite challenging.

Parameter	***Value***
Resolution	14 bit
Bandwidth	5 MHz
Center frequency (*IF*)	20 MHz
Sampling frequency	80 MHz
Signal-to-noise and distortion ratio (*SNDR*)	80 dB
Spurious-free dynamic range (*SFDR*)	90 dB
Input voltage range	1 $V_{pp,\,diff}$

Table 1. *Specifications of an A/D converter for third generation base transceiver stations*

2. A/D CONVERTER ARCHITECTURE

MASH architectures [2, 3] ideally allow the actual order of the ΣΔ modulator loops to be reduced without loosing the high-order noise shaping effect or the equivalent resolution of the quantizer to be increased without introducing linearity problems. In particular a MASH *L*-0 architecture, consisting of an *L*-th order ΣΔ modulator followed by an *N* bit pipeline A/D converter, as shown in Fig. 1, appears very promising for the considered applications [4].

In this architecture, the quantization noise of the ΣΔ modulator, converted into the digital domain by the pipeline ADC, is subtracted from the output of the ΣΔ modulator, after being filtered by a digital replica of the ΣΔ modulator noise transfer function, leading to

$$\begin{aligned} Out &= STF(z)In + NTF(z)\varepsilon_{\Sigma\Delta} \\ &\quad - (\varepsilon_{\Sigma\Delta} + \varepsilon_{PL})NTF_D(z) \\ &= STF(z)V_{in} + \varepsilon_{PL}NTF(z) \end{aligned} \quad , \qquad (1)$$

where $\varepsilon_{\Sigma\Delta}$ and ε_{PL} denote the quantization noise of the ΣΔ modulator and of the pipeline converter, respectively, while $STF(z)$ and $NTF(z)$ represent the signal and noise transfer function of the ΣΔ modulator.

If the digital replica $NTF_D(z)$ of the noise transfer function matches $NTF(z)$, the MASH structure features the same noise characteristics of a ΣΔ modulator having the noise shaping given by $NTF(z)$ and an internal quantizer with resolution given by the sum of the resolutions of the pipeline ADC and of the ΣΔ modulator internal quantizer.

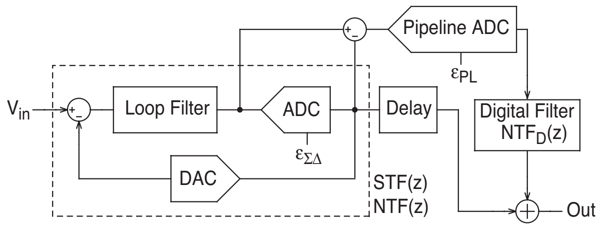

Figure 1. *A/D converter based on the MASH L-0 architecture*

Therefore, the benefits of a MASH architecture with respect to a multi-bit ΣΔ modulator are relevant. In a multi-bit ΣΔ modulator, the errors introduced by the DAC required in the feedback loop are treated exactly as the input signal, causing, if robust digital correction techniques are not applied, a drastic reduction of the achievable performance, both in terms of *SNDR* and *SFDR*.

In fact, it can be demonstrated that, in multi-bit ΣΔ modulators, the non linearity of the DAC causes harmonic distortion and an increase of the in-band noise due to intermodulation of high-frequency harmonic components.

By contrast, with the proposed MASH architecture, any error introduced by the pipeline converter is attenuated, in the band of interest, by the digital replica of the ΣΔ modulator noise transfer function. More importantly, the pipeline converter does not produce any harmonic distortion, because its input is the quantization noise of the ΣΔ modulator, which is substantially uncorrelated from the MASH input signal.

Furthermore, in a single-stage ΣΔ modulator, since the quantizer is included in the feedback loop, an increment of its resolution has to be obtained without changing its delay, not to modify the loop filter transfer function. This, usually, implies the use of a parallel (“flash”) quantizer, with its well-known drawbacks in terms of area and power consumption. By contrast, in a MASH *L*-0 A/D converter, it is possible to use a single bit quantizer in the ΣΔ modulator, thus avoiding the linearity problem typical of multi-bit systems previously discussed, and to obtain at the same time the advantages of multi-bit converters, by properly choosing the second stage resolution.

Since the second stage is outside the ΣΔ modulator feedback loop, it can be implemented using any architecture, independently of its delay. If we use a pipeline A/D converter, obviously we have to compensate its latency with a matched delay (typically a shift register) connected at the output of the ΣΔ modulator (Fig. 1). Additionally, the absence of constrains on the converter latency allows the use of redundancy in the pipeline stages, improving the robustness of the overall architecture.

3. A/D CONVERTER IMPLEMENTATION

In this paper we propose a bandpass A/D converter based on a MASH 6-0 architecture, whose block diagram is shown in Fig. 2. The circuit consists of a 6-th order bandpass ΣΔ modulator with a 1.5 bit quantizer (equivalent to a 3-rd order lowpass modulator), followed by a 10-bit pipeline ADC with 1.5 bit per stage and digital error correction (DEC).

The use of a 1.5 bit quantizer in the ΣΔ modulator grants two fundamental benefits. Firstly, it allows us, as in the case of the single bit quantizer, to achieve excellent linearity without requiring matched components. Moreover, the use of a three level quantizer allows us to introduce, in the overall converter, some redundancy, relaxing the constrains on the required threshold levels.

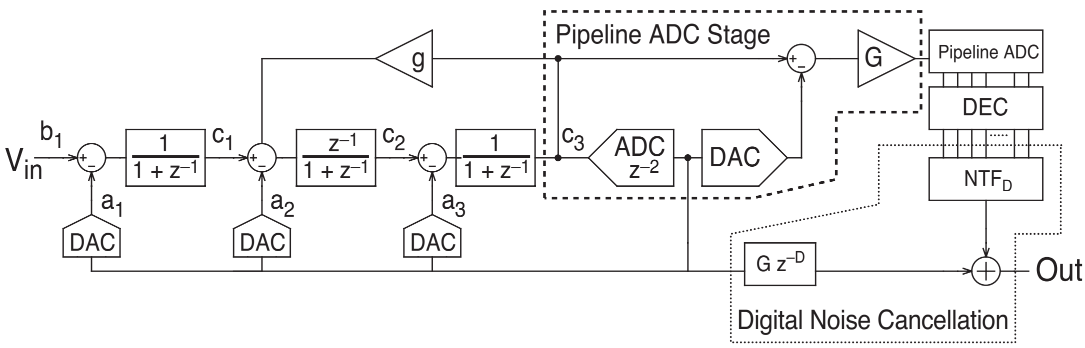

Figure 2. *Proposed A/D converter architecture*

The noise transfer function of the ΣΔ modulator has been optimized to minimize the quantization noise in the 5 MHz bandwidth, leading to

$$\begin{aligned} NTF(z) &= \frac{1 + 2.9z^{-2} + 2.9z^{-4} + z^{-6}}{1 + 2.15z^{-2} + 1.65z^{-4} + 0.45z^{-6}} \\ STF(z) &= \frac{-0.05z^{-4}}{1 + 2.15z^{-2} + 1.65z^{-4} + 0.45z^{-6}} \end{aligned} \quad . \qquad (2)$$

The corresponding values of the ΣΔ modulator coefficients are: $a_1 = 0.5$, $a_2 = 0.2$, $a_3 = 0.75$, $b_1 = 0.5$, $c_1 = 0.1$, $c_2 = 1$, $c_3 = 1$ and $g = 0.1$.

The pipeline ADC consists of eight stages resolving 1.5 bits each and one stage resolving 2 bits. The schematic of the 1.5-bit pipeline stage is illustrated in Fig. 3 [5]. During clock phase 1 the input signal is sampled onto capacitors C_f and C_s connected in parallel and by the 1.5-bit flash ADC. During clock phase 2 capacitor C_f is connected in feedback around the operational amplifier, while capacitor C_s is connected by the DAC switches either to $+V_{ref}$, $-V_{ref}$ or zero, depending on the output of the ADC.

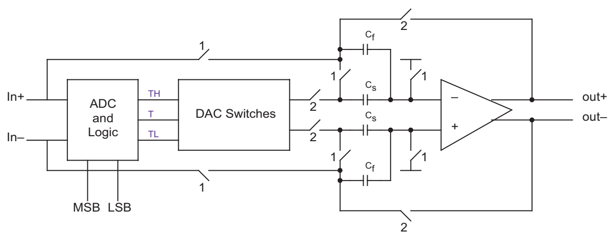

Figure 3. *Schematic of the 1.5 bit pipeline stage*

The MASH A/D converter has been realized with the switched-capacitor technique using the single operational amplifier resonators illustrated in Fig. 4.

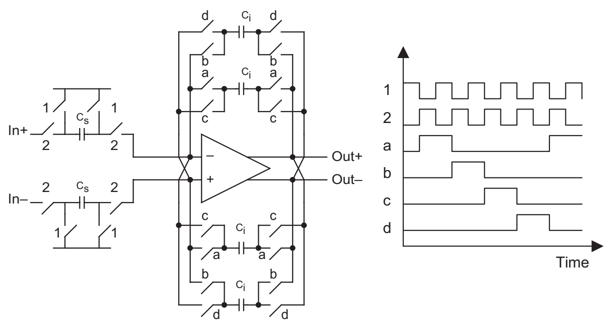

Figure 4. *Schematic of the single operational amplifier resonator used*

In this structure the resonator transfer function

$$R(z) = -\frac{C_s}{C_i}\frac{1}{1 + z^{-2}} \qquad (3)$$

is obtained using two different integration paths sharing the same operational amplifier. This system allows, of course, power consumption saving, but can suffer from mismatches between the paths. In fact, odd and even samples are integrated, using the same operational amplifier, on different capacitors (with the same nominal value).

Nevertheless, extensive Monte Carlo simulation have confirmed that realistic mismatch among capacitors does not influence the overall converter resolution. In higher resolution applications the problem could become more significant and the use of two operational amplifier resonators is recommended.

The operational amplifier used is based on a two stage architecture with Miller compensation.

4. Simulation Results

The proposed circuit has been extensively simulated, both at behavioral level and at circuit level. The power spectral densities (*PSD*) of the ΣΔ modulator and of the MASH structure, as well as the *SNR* as a function of the signal amplitude are shown in Fig. 5.and in Fig. 6, respectively.

Particular attention has been taken to understand the effect on the converter behavior of differences between the actual coefficients values and the ideal ones. The proposed structure has shown a good robustness against errors as large as 0.1%. For larger errors the difference between the effective ΣΔ modulator noise transfer function and its digital replica becomes relevant, reducing the resolution to less than 12 bits for 1% errors.

If required, in order to maximize the matching between *NTF* and NTF_D, an adaptive filter can be used to implement NTF_D. The adaptation can be performed by injecting a pseudo-random test signal at the input of the ΣΔ modulator quantizer, extracting its power at the output by correlation with the same pseudo-random sequence and using the LMS algorithm to vary the digital filter coefficients in order to minimize it, as shown in Fig. 7 [6, 7, 8].

5. Conclusions

In this paper a two stage bandpass MASH ΣΔ modulator has been presented. A resolution of 14 bits has been achieved over a 5 MHz band around an IF of 20 MHz with a clock frequency of 80 MHz. This performance has been obtained using a 6-th order bandpass ΣΔ modulator followed by a 10 bit pipeline converter. The simulation results achieved demonstrate the validity of the proposed approach, making this solution very attractive for the im-

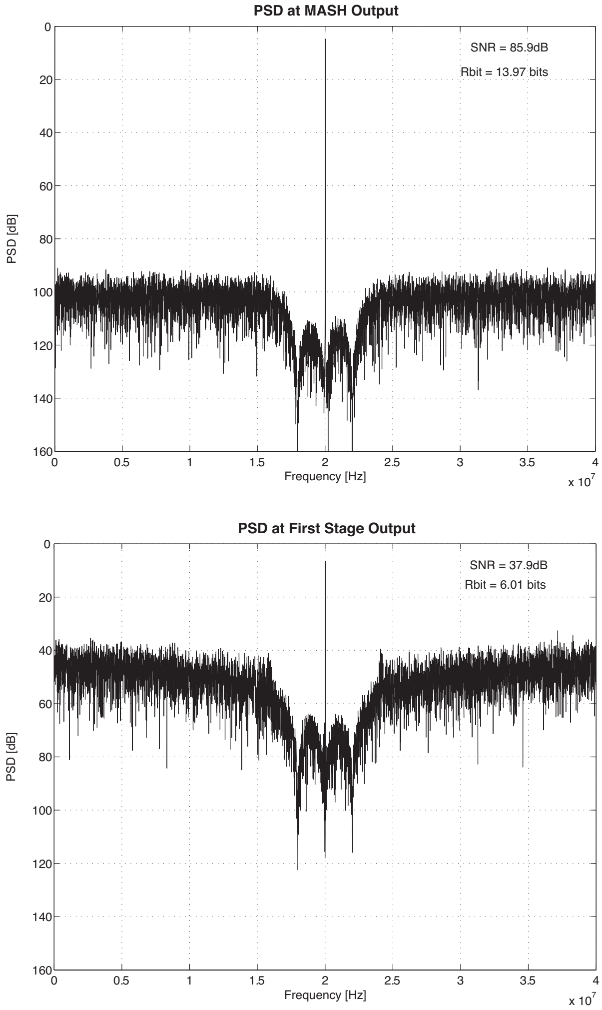

Figure 5. *PSD of the ΣΔ modulator and of the MASH structure,*

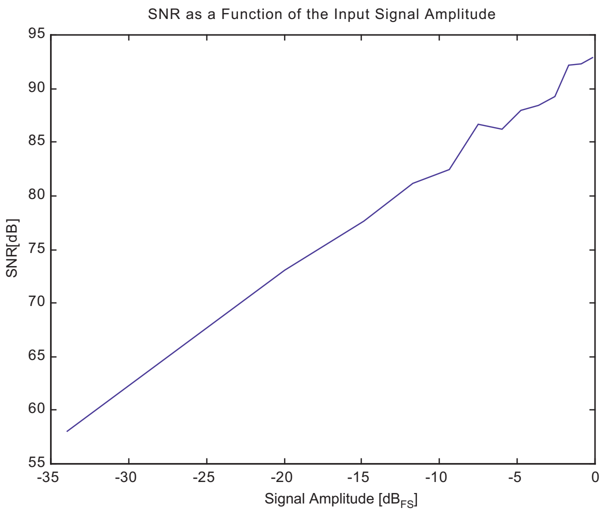

Figure 6. *SNR as a function of the signal amplitude of the proposed A/D converter*

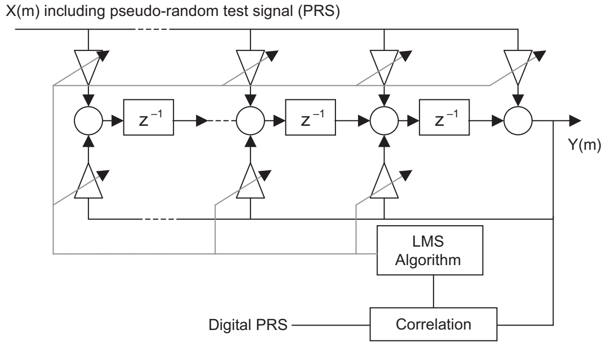

Figure 7. *Coefficient mismatch cancellation technique*

plementation of the A/D converters for IF sampling in third generation telecommunication systems.

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