A/D converter in superconductor-semiconductor hybrid technology

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Abstract - Josephson junctions can act as fundamentally accurate voltage-to-frequency converters, and niobium-based superconductor A/D converters (ADCs) have therefore been show-cases for superconductor electronics. But the need for cooling to liquid helium temperature (of 4K) has so far precluded any commercial applications.

In the European project SUPER-ADC (IST 2001-33468) an alternative "high-temperature" superconductor approach is being pursued: a hybrid ADC, in which a high-Tc superconductor delta-sigma modulator is interfaced with a CMOS decimation filter. This approach takes advantage of the very high over-sampling rate and fundamental exactness of a high-Tc super-conductor delta-sigma modulator, and the outstanding capability of CMOS technology for complex filtering. The "penalty" is an interface, which has to bridge a (mV-to-V) voltage and a (20GHz-to-1GHz) speed mismatch, besides a 30K to room-temperature difference.

This presentation describes, briefly, the underlying surprisingly simple superconductor "rapid single flux quantum" (RSFQ) technology, and some of the details of the hybrid ADC realization.

Keywords - RSFQ, superconductor delta-sigma modulators, hybrid ADC

I. INTRODUCTION

The development curve for semiconductor A/D converters (ADCs) indicates that conventional ADCs, delivering 16 effective bits spurious-free dynamic range (SFDR) at 60 MHz analog input band-width, which are immediately needed for advanced radar and wide-band mobile radio communication systems, will not exist within the next 10-15 years [1, 2]. It is the aim of the EU project SUPER-ADC (IST 2001-33468) to demonstrate a superconductor-semiconductor hybrid ADC of such performance by 2004.

The SUPER-ADC project started Jan 1, 2001 and will finish Dec 30, 2004. The participants are Chalmers University of Technology (SE), the University of Twente (NL), the Gerhard Mercator University of Duisburg (DE), Thales Technologies (FR), Air Liquide (FR) and Infineon Technologies (SE). (See www.super-adc.org .)

ADCs of the Delta-Sigma type are ideal for implementation in superconductor so-called Rapid Single Flux Quantum (RSFQ) technology. This technology is based on the exact magnetic flux quantization in (small) superconducting loops, in which Josephson junctions acts as gates for shuttling flux quanta in and out of the loops. RSFQ logic is, simply, a logic network of such loops and Josephson junctions, characterized by very high speed and extremely low power consumption as compared to conventional semiconductor logic [3]. RSFQ is capable of huge over-sampling rates and also to provide exact cancellation (D/A conversion) in the feedback loop of the DS modulator. Besides, the RSFQ modulator is surprisingly simple compared to its semiconductor counterpart.

Niobium superconductor ADC chips have been shown to be clearly superior to their semiconductor counterparts, even in very primitive (3.5 micron line-width) implementations. From the user point of view, however, their need to be cooled to liquid helium temperature have precluded any civilian applications. ADCs based on the recent "high-temperature" superconductor (HTS) technology would be a great leap forward, as they would require comparatively simple coolers and be "temperature compatible" with existing HTS microwave components such as HTS filters and phase-shifters. (In addition, as the energy gap of HTS is about 100 times larger than that of Nb, they would in principle be 100 times faster than the ones made of Nb.) Monolithic ADC chips based on HTS are, however, completely out of reach of present HTS (materials) technology. The complex digital decimation filter part of the ADC, following the over-sampling sigma-delta modulator, will have to be made in CMOS. The real challenge for the EU project is to bridge the speed and voltage mismatch between the HTS modulator and the CMOS filter.

II. HYBRID ADC ARCHITECTURE

Given the overall requirements, and the technology limitations, we arrived at the ADC architecture outlined in the block diagram below.

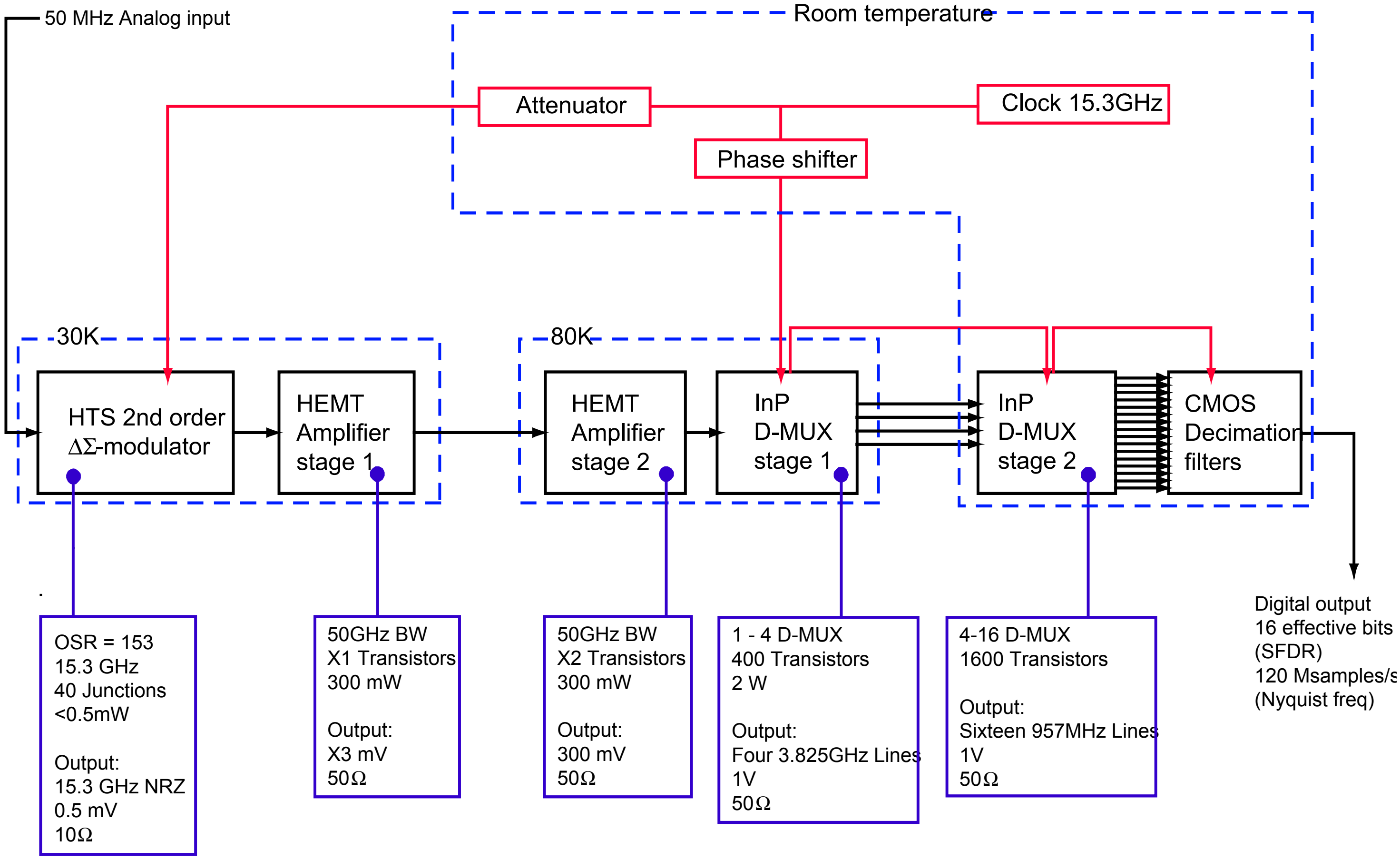

Fig. 1. Block diagram of the proposed superconductor-semiconductor hybrid ADC

III. THE MODULATOR

Delta-sigma modulators are surprisingly simple devices in RSFQ technology. A superconducting inductor integrates the signal and a Josephson junction provides the comparator and the feedback functions; an exact number of flux quanta are being fed back [4]. And because of the sub-pico-second sampling capability of the Josephson junction, there is in practice no upper limit to the over-sampling ratio (OSR). The requirement of 16 effective (SFDR) bits can be fulfilled by a 1st order delta-sigma modulator with an OSR of 2416, or a 2nd order delta-sigma modulator with an OSR of 153. For a 50 GHz analog signal this means a sampling clock frequency of 241 GHz for a 1st order modulator, and 15.3 GHz for a 2nd order modulator [5]. Clearly, only the second alternative can be handled by a semiconductor interface. The 2nd order modulator would contain 40-50 Josephson junctions, which is bordering the capability of next year's HTS technology. (University of Twente and Chalmers have HTS circuit fabrication capability of about 10-20 Josephson junctions with 1σ spread in critical current density of about 10-20%. The goal is to develop the technology, to allow fabrication of 40-50 junctions with 1σ spread in critical current density of < 8%).

IV. CRITICAL PARTS OF THE INTERFACE

A critical part of the HTS-CMOS interface is the high-speed semiconductor amplifier needed to amplify the digital mV-level signal coming out of the HTS modulator. To feed the InP digital (demultiplexer) circuitry with adequate signals, the amplifier should have a gain of about 50 dB over a bandwidth approaching 50 GHz. Such demands inherently lead to potential stability problems. To combat this, the amplifier has been divided into two sub-circuits, AMP1 and AMP2, as shown in the block diagram. (This division will also relax the cooling requirements on the 30 K stage.)

The InP High Electron Mobility Transistors (HEMTs) represent the state-of-the-art in terms of maximum frequency of oscillations (>600 GHz) and noise figure (of the order 1 dB at 100 GHz) for any semiconductor device. Due to the combination of high electron mobility and velocity, the drain current is saturated at a quite small voltage, of the order 0.1-0.3V. The device is therefore an interesting one for cryogenic applications, where the cooling load is a concern.

A word on the interconnect problem of the 30K module: The amplifier must also be able to cope with an input impedance of 10 ohms from the HTS circuit. The impedance mismatch between the HTS and the semiconductor circuits stem from the fact that the Josephson junctions have a critical current – normal resistance product, $I_cR_n = 1$ mV (determined by the HTS technology). With $I_c = 100$ μA (determined by noise limit requirements), this leads to $R_n = 10\ \Omega$, well below the standard interconnect impedance of 50 Ω. A wide-band impedance transformer would occupy a lot of real estate, which is impractical both for the HTS and InP chips; an MCM carrier or a large chip-bridge could be used for it.

V. THE COOLING ISSUE

The size, efficiency and cost of the cooler is crucial for the commercial acceptance – overcoming the "cryophobia" of the industrial user. The aim is therefore to improve existing single-stage Stirling cooler performance for a few watts at 80 K to about 300 mW at 30 K. (It should be pointed out that such coolers did not exist at the outset and that such coolers are being successfully developed within the project.) Very compact and efficient single-stage pulse-tube coolers for more than 6 W of cooling capacity at 80 K has been developed. A 30K stage is feasible within the same pulse-tube technology; a much simpler design than that of a comparable Stirling cooler.

V. QUESTION MARKS

The ADC architecture is clearly open to technological changes during the course of the project; something we have referred to as it being "future proof". The 16 (effective) bits output is a primary objective; the input signal band-width requirement (of 60 MHz) may be relaxed in the first "iteration". As pointed out, a 2nd order RSFQ delta-sigma modulator will require about 40 Josephson junctions, and the InP DMUX about 1000 transistor functions, both of which slightly beyond the HTS and InP technology at the start of the project, but expected to be feasible towards the end of it.

Another, very important question-mark is on the future of (cryo-) CMOS: Will it in the end be possible to simply cool the CMOS front-end of the decimation filter to speed it up sufficiently for us to discard the InP demultiplexers?

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